SYNTHESISED FREQUENCY SOURCES IN DIGITAL CELLULAR HANDSETS

G Smithson, Plextek Ltd, London Road, Great Chesterford, Essex. Tel 01799 533255. gs@plextek.co.uk

The design and implementation of high performance synthesised frequency sources is key to the operation of digital cellular phones. This paper considers the simulation and design of synthesiser solutions including analysis of the performance requirements such as switching speed, phase noise and stability margins. The principles of operation of a synthesiser are considered along with the design of the loop filter.

Once designed the implementation of a synthesiser system in a cellular handset contains many potential pit falls. These include phenomena such as the 'pulling' of the oscillator's frequency due to RF feedback, changing antenna VSWR and via the power supply.

SYNTHESISER SYSTEM

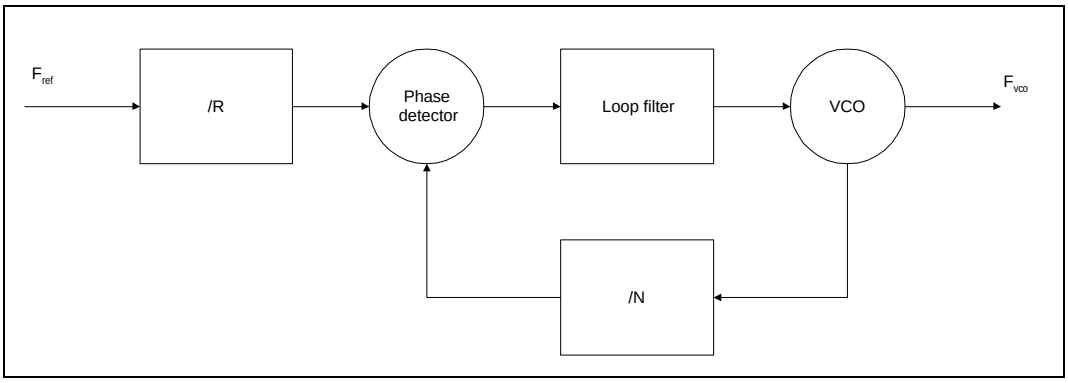

Fig 1 Synthesiser system block diagram.

The block diagram of a generic single loop phase locked synthesiser system is shown in Fig 1 above. While the exact implementation can vary, the principle method of operation remains the same. This involves dividing a reference signal (typically derived from a crystal based oscillator) by a programmable integer R, the VCO signal by a programmable integer N and then comparing the phase of the two signals and generating an error signal accordingly. The desired lock frequency is then given by:-

$$f_{vco} := \frac{N}{R} \cdot f_{ref}$$

LOOP FILTER REALISATION

Different synthesiser devices support different options for the loop filter. These broadly speaking fall into two categories; voltage proportional outputs and charge pump outputs. The voltage proportional output types are typically used in conjunction with low 1/f noise op amps configured as integrators. One advantage of this system is the flexibility to operate the loop filter from a power supply totally independent of the synthesiser device. This will usually allow a reduction in oscillator Kvco and generally make the oscillator design simpler if a suitable supply exists (for instance 12V). The disadvantage of this configuration is that the 1/f noise of the op amp will modulate the VCO and potentially result in increased phase noise.

The type of synthesiser most commonly used in modern cellular phones employs digital charge pumps. Typically these operate by having two current sources, one to push current out and one to suck current in. Depending on whether the phase of the reference leads the phase of the feedback or vice versa one of the current sources is fired for a duration proportional to the phase error. If the phase and frequency are locked neither current source will fire and the PLL output will remain in a high impedance state. The principle advantage of this type of arrangement is that when the system is locked all active circuits connected to the loop filter are

turned off with the varicap voltage simply held as charge in a capacitor. This minimises the additional phase noise contributed by the loop filter output voltage, although the use of large value resistors in the filter must be treated with care as this can potentially increase phase noise due to the thermal noise voltage developed. The theoretical operation of the current sources is shown in Fig 2a,b and c below.

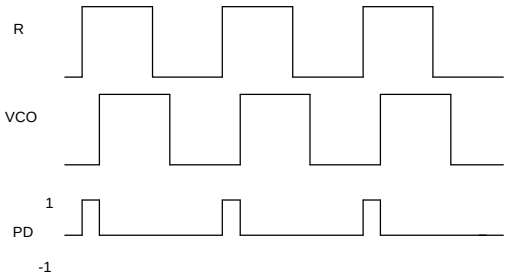

Fig 2a Reference leading VCO

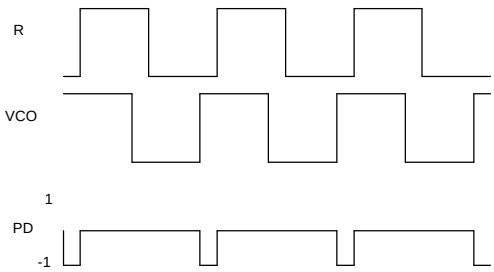

Fig 2b Reference lagging VCO

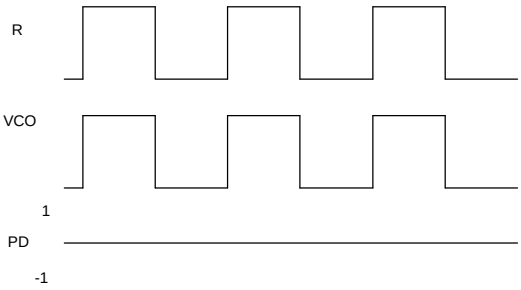

Fig 2c Phase and Frequency locked

Due to the domination of the charge pump type of PLL in modern mobile and cellular products only this type will be considered further.

CHARGE PUMP PLL LOOP FILTER

Fig 3 below shows a typical realisation of a third order loop filter with resistive coupling to the varicap. (The time constant of R4 and Cv are assumed to have a negligible effect on the dynamics of the loop).

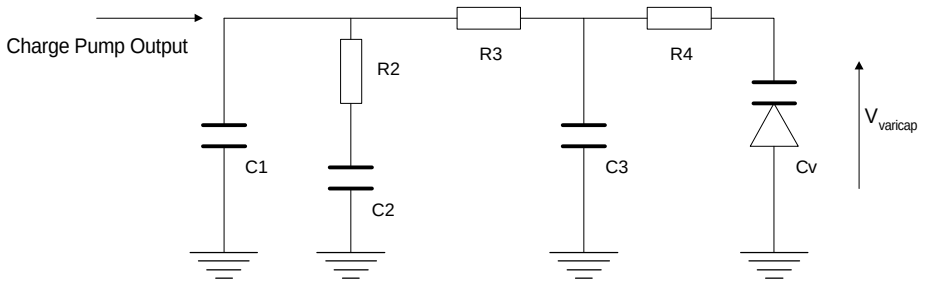

Fig 3 Typical loop filter configuration.

S - DOMAIN TRANSFER FUNCTION

In order to design and simulate the system, linear control theory can be used to derive a transfer function for the loop. Using the s domain transfer functions of the forward and reverse elements the system can be represented as:-

$$T(s) := \frac{G(s)}{1 + G(s) \cdot H}$$

where

$$G(s) := K\phi \cdot Z(s) \cdot \frac{Kvco}{s}$$

and

Kϕ := Phase detector gain
Z(s) := Loop filter transfer function
Kvco := VCO gain
H := 1/N

The open loop transfer function, G(s).H, will be used to assess the loop stability and bandwidth in the practical design example given below. When using the equations above it is very important to use the correct units. Typically Kϕ will be in A/2π radians, Z(s) in V/A, Kvco in Hz/V and H is simply a ratio having no units.

CASE STUDY:- 900 MHZ GSM SYNTHESISER SYSTEM DESIGN

The principle objective of the PLL system used for the up/down conversion in a cellular phone is usually to lock a relatively low Q VCO with a relatively wide tuning range to a high stability, high Q reference. The principle reasons for employing closed loop synthesis being to both allow accurate channel selection and to reduce the phase noise of the VCO within the loop bandwidth. The selection of the R and N divider are then used to select the required channel.

When commencing the design of a synthesiser system the following requirements must be identified; frequency range, channel separation, phase error, switching time, spurious outputs and the VCO characteristics. For the following case study we will assume these requirements, as consistent with an on frequency transmit VCO for a 900 MHz GSM phone:-

Frequency range:	890 - 915 MHz
Channel separation:	200 kHz
Phase error:	1^o rms. *
Switching time:	500 us **
Spurious outputs:	-60 dBc
VCO characteristics:	12 MHz/V

* Typically the contribution associated with the UHF VCO.
** Assumes that this VCO is shared with the receiver circuitry.

LOOP DYNAMICS

As a general rule the higher the comparison frequency the better. Typically this will result in a shorter switching time, lower close in phase noise and lower reference sidebands. A rule of thumb for equating the switching speed of a synthesiser to the comparison frequency is that at least 50 comparison periods will be required to settle the VCO. A second rule of thumb for relating a required switching speed to the loop natural frequency is that typically a switching speed of 2.5 x the reciprocal of the natural frequency can be achieved. For this case study these two rules of thumb yield a suggested natural frequency of > 5 kHz and a required comparison frequency of > 100 kHz. As a comparison frequency equal to the channel separation (200 kHz for the GSM system) is convenient, this is chosen.

The damping characteristics of the loop requires careful consideration as this will have a strong influence over the switching time. Considering the scenario where an oscillator locked at 892 MHz is commanded to change frequency to 910 MHz. At the instance the N divide is changed the VCO feedback signal at the phase detector

will lag the reference signal. Initially, prior to the increase in the varicap voltage, the phase error will increment by approximately 7^o per comparison period. Optimum switching time will not allow a 360^o slip of phase to occur therefore the frequency of the VCO must be increased, not only to achieve frequency lock, but also to accrue the slipped phase so that the lock conditions defined in Fig 2c can be achieved. Only then will phase and frequency lock have been achieved.

To summarise; In order to simultaneously achieve phase and frequency lock with a synthesiser performing a fast step frequency jump, as described above, it is necessary for the frequency response to overshoot. Typically a damping factor of between $1/\sqrt{2}$ and 0.5 is optimum, yielding the best compromise between rapid convergence of phase and frequency and fast setting of the switching transient. The requirement to overshoot means that the VCO must have considerably more tuning range that would at first appear necessary, typically an additional 50%.

PHASE ERROR

The requirement, as defined in the GSM 05.05 specification, is that the total transmit phase error should be less than 5^o rms. The primary causes of phase error in the transmitter are the modulator, the steady state oscillator phase noise, power amplifier AM to PM conversion and PA switching transients. A budget of 1^o rms. for the 900 MHz VCO is reasonable. Using the equations in ref. [3] for equating the energy in the sidebands to the energy in the carrier yields a required maximum sideband energy of approximately -38 dBc. Therefore the integrated sum of all the energy in the sidebands must be 38 dB less than the energy in the carrier for a phase error of 1^o rms.

CALCULATION OF COMPONENT VALUES

The process of calculating the loop component values can be conveniently performed on a computer in a package such as Excel or MathCad. Additionally this can be combined with the plotting of the open loop Bode plots to allow the gain and phase stability to be assessed. An in-depth analysis of the equations for deriving the component values can be found in reference [1] or [2].

From analysis in ref. [1] the following equations can be used to calculate the component values:-

$$C2 := \frac{Kvco \cdot Icp}{\omega n^2 \cdot N} \qquad C1 := \frac{C2}{12} \qquad R2 := 2 \cdot \rho \cdot \sqrt{\frac{N}{Kvco \cdot Icp \cdot C2}}$$

$$R_3 := 3 \cdot R_2 \qquad C_3 := \frac{R_2 \cdot C_2}{\left(20 \cdot R_3\right)}$$

Where ωn is the natural frequency in rad/s, Icp in A/cycle and ρ is the damping coefficient. From the analysis of the system requirements above Kvco = 12 MHz/V, $\rho = 0.707$, $\omega n = 2\pi.5000$, N = 4512 and Icp = 2 mA.

C1 = 470pF	C2 = 5.6nF	C3 = 82pF
R2 = 8.2k	R3 = 22k	R4 = 10k

OPEN LOOP GAIN AND PHASE BODE PLOTS AND STABILITY MARGINS

Once the component values have been determined the gain and phase margins should be analysed to ensure stable closed loop operation. The gain margin is defined as the amount of additional open loop gain that would be required to satisfy the conditions for oscillation, i.e. 0^o phase shift and unity gain. From Fig 4b below it can be seen that the open loop transfer function has 180^o phase shift at approximately 55 kHz. As the phase detector

effectively adds 180^o phase shift to the open loop transfer function (due to the subtraction at the phase detector), the additional gain required for unity gain at this frequency is the gain margin. Inspection of Fig 4a shows this is approximately 22 dB. Typically a value greater than 15 dB should be sufficient.

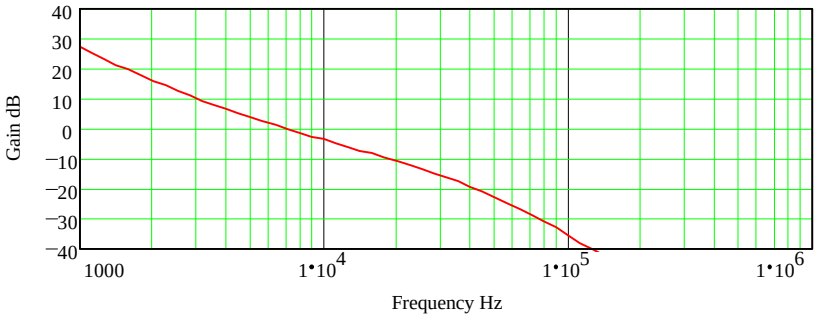

Fig 4a Open loop Gain Bode plot.

In addition to considering the gain margin the phase margin should be analysed to ensure stability. The phase margin is defined as the amount of additional phase shift that would be required for the open loop transfer function to satisfy the conditions of oscillation, i.e. 0^o phase shift and unity gain. From inspection of Fig 4a it can be seen that unity gain occurs at approximately 7 kHz. Analysis of Fig 4b shows that an additional 50^o phase shift would be required to satisfy these conditions. Typically a phase margin in excess of 30^o is sufficient.

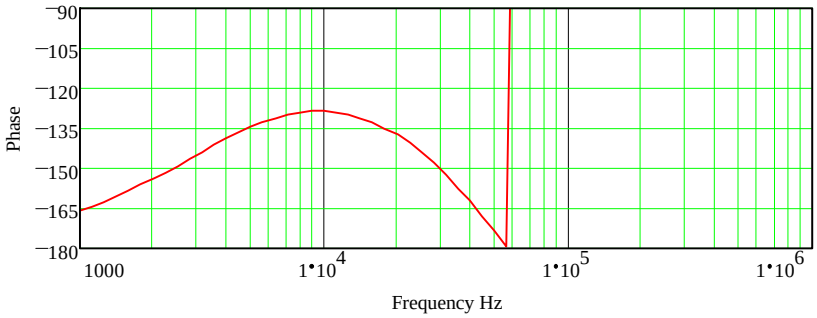

Fig 4b Open loop Phase Bode plot.

TIME AND FREQUENCY DOMAIN SIMULATION OF A SYNTHESISED SOURCE

Once the stability has been checked the dynamics of the loop can be simulated. The two principle characteristics of interest are switching time and phase noise, although reference sideband levels can also be important. Fig 5 below shows the results of a time domain simulation of the switching transient. The transients caused by the action of the charge pump can clearly be seen as the voltage across C1 increases and then decreases as some of the charge flows through R2 into C2.

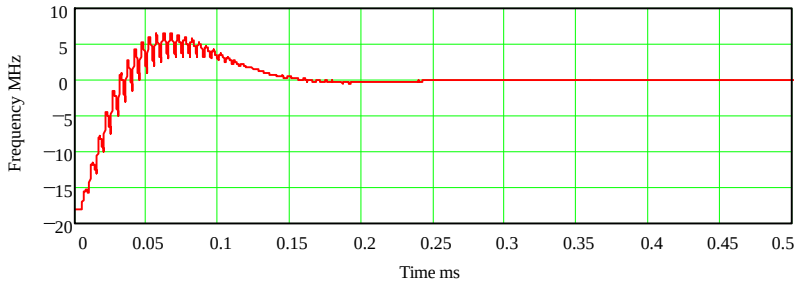

Fig 5 Switching transient simulation.

Simulation of the anticipated phase noise spectra can be performed in various ways. The simplest method is to split the spectra into three regions; reference oscillator noise, phase detector noise floor and oscillator phase noise. These three regions can be seen in Fig 6 below. The phase noise close in to the carrier is dominated by the reference oscillator phase noise increased by the multiplication factor (20.LOG N/R). The mid frequency section of the PLL spectra is dominated by the phase detector noise floor, increased by the multiplication factor (20.LOG N). At frequencies greater than the loop bandwidth the noise of the spectra will be dominated by the VCO phase noise. For synthesiser devices such as the Siemens PMB2307 or Philips UMA1021 a noise figure of approximately 15 dB is a reasonable assumption.

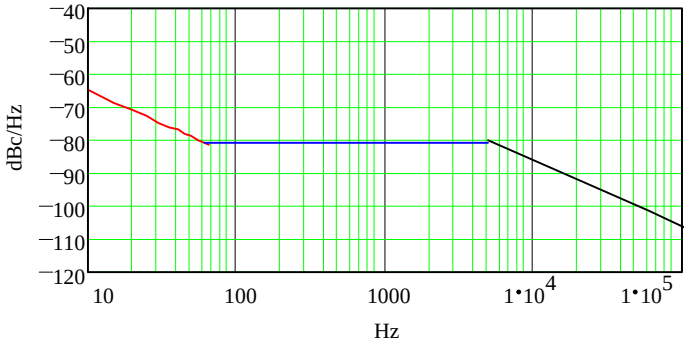

Fig 6 Phase noise simulation.

The integrated sum of the phase noise shown in Fig 6 is approximately < -38 dBc.

MEASURED RESULTS

The PLL system designed above has been built and the resultant spectra is shown in Fig 7 below. The measured spectra shows good correlation to the simulations above.

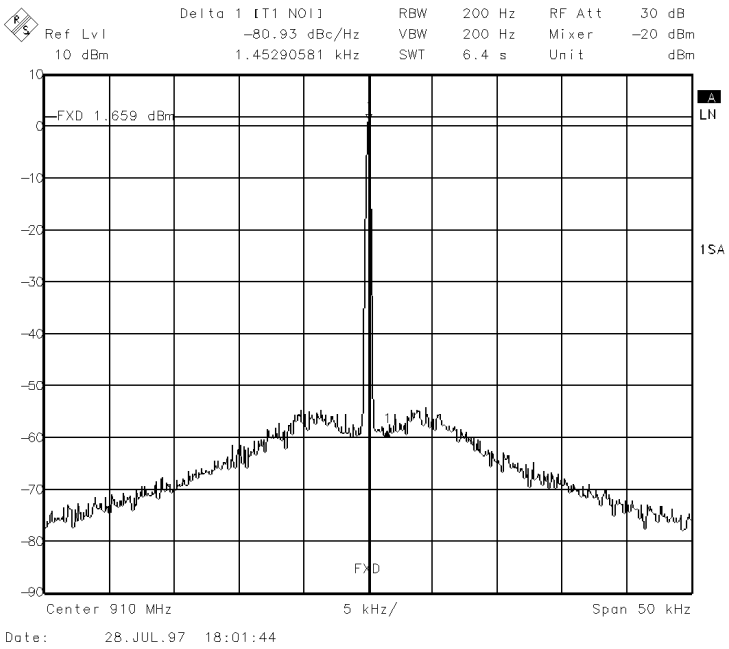

Fig 7 Measured Phase noise spectra.

SYNTHESISER SYSTEM IMPLEMENTATION

The design of a synthesiser system as discussed above is only the first step in implementing a synthesised VCO in a real product. Once built various practical problems can be encountered, the most common one of these is pulling of the frequency by an external influence such as a dip in the power supply voltage. In a TDD system, such as GSM, the internal resistance of the battery and the battery tracks on the PCB can result in a dip in the supply when the PA is switched on. Typically a separate regulator would be used for the VCO, although the finite load regulation of these devices can still result in a frequency transient.

A similar effect can be produced if there is a variation across the ground plane on the board, particularly when a potential difference is developed between the ground on the varicap diode and the ground on the loop filter capacitors. Careful layout is required to minimise any potential differences, especially when large currents are being drawn by the PA.

The final two potential causes of frequency pulling that are considered are load pulling and RF feedback. The VCO will be susceptible to any change in impedance at its output. Additionally the frequency of the oscillator can be pulled if large amounts of RF signal are injected into the VCO tank circuit. This phenomena is considerably worse if the oscillator is on the same frequency as the fedback signal. To try and minimise these two effects multiple stages of active buffering as well as RF screening around the VCO tank are typically implemented. Alternatively the significance of these mechanisms can be reduced by using a superhet transmit architecture so that the oscillator is no longer ‘on frequency’.

References.

[1] Philips Semiconductors; Application Note: UMA1018M synthesiser Report N^{o}: AN94003; 10th February 94; page 32.

[2] Siemens Semiconductors; Using Excel to design a loop filter for a PMB2307 Phase Locked Loop IC or equivalent; Application hints Version 9; September 95; page 13 - 17.

[3] Constantine Fantanas; Introduction to phase noise; RF Design; Aug 92; page 50.

General Reference.

[4] Gardener; Phaselock Techniques; Wiley-Interscience; 1979