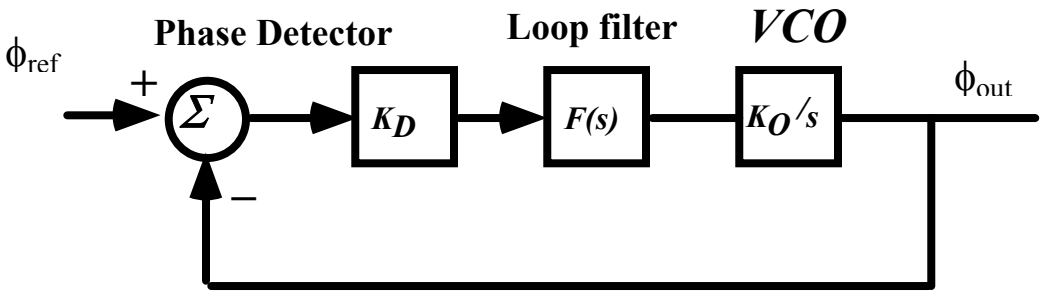
Frequency Synthesis – PLL

Reading: Motorola AN 535 and Manassewitsch (both in reading supplement)
Lee, Sect. 16.7



A phase locked loop is a feedback system that includes a VCO, phase detector, and low pass filter within its loop. Its purpose is to replicate the input frequency and phase on the output of the VCO when in lock. The phase detector produces an error voltage in proportion to the phase difference between the reference and VCO signals.

Frequency synthesizers use a PLL to copy, multiply, or divide a crystal reference source. The stability and phase noise properties of the crystal reference oscillator are preserved within the loop bandwidth of the PLL.

ϕ_{ref} = input reference phase.

- Usually from a crystal oscillator.

ϕ_{out} = output phase from VCO

$\phi_{out} = \phi_{ref} + \text{const.}$

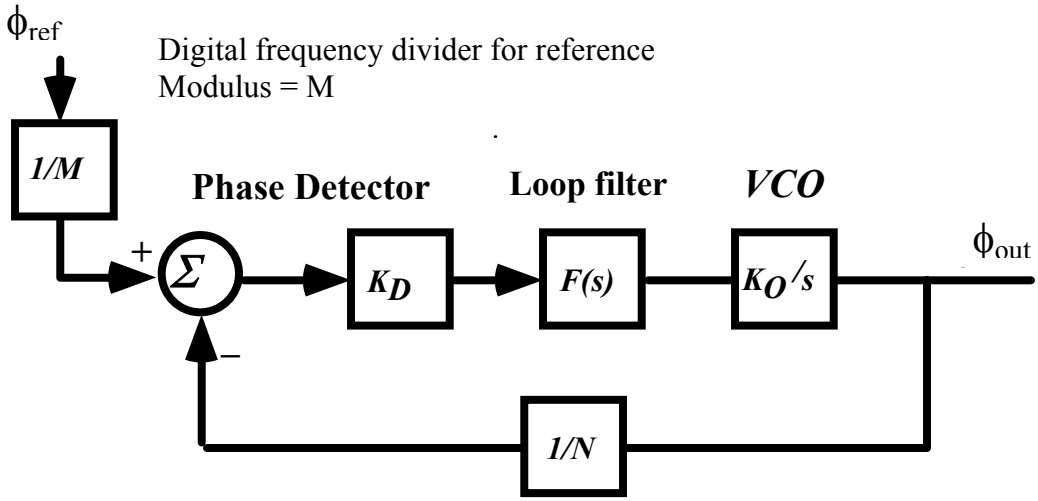
- Output phase is tracking input phase when loop is locked.

$\omega_{out} = \omega_{ref}$

- Output and input frequencies are the same when feedback factor = 1.

Loop filter: stabilizes loop. Establishes bandwidth of PLL and controls pull-in time required for loop to stabilize after a frequency change.

An output frequency that is a multiple of the reference frequency can be obtained if digital frequency dividers are included in the reference and VCO feedback path. The phase detector will keep the frequencies equal at its inputs and track the phases.



The output frequency is adjustable using digital variable modulus frequency dividers on the reference and VCO paths to the phase detector.

$$f_{out} = f_{ref} N/M$$

Thus, a tunable frequency source is available which has phase locked to a reference source and whose stability is similar to a fixed frequency crystal oscillator. For this structure, the frequency step size is f_{ref}/M.

How does the design of the frequency synthesizer differ from the FM Demodulator?

	FMD	FS
Input level	Can have low S/N	You choose the S/N for best performance. Crystal oscillator may have 100 dB S/N
Function	Tracking of frequency	Frequency up/down conversion
We want	Low THD Low noise	Low phase noise
Loop BW	Narrow – similar to IF bandwidth	As wide as possible while preserving low spurious outputs
Transfer function	$V_O(s)/\omega_{in}(s)$	$\phi_{out}(s)/\phi_{in}(s)$

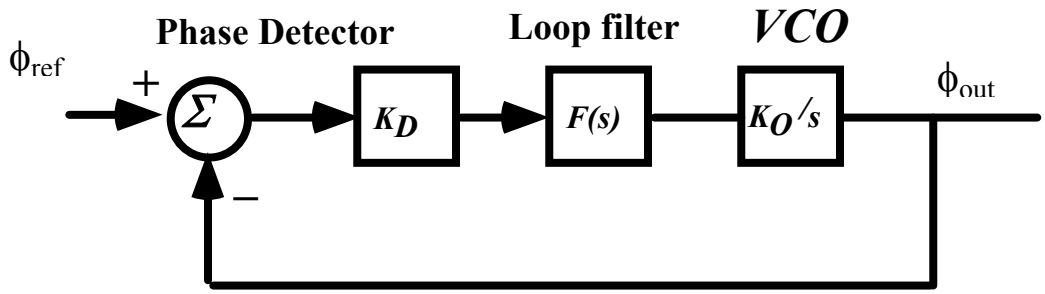
The frequency synthesis application is concerned with:

1. Transient response to a frequency step
2. Steady state phase error for frequency step
3. Stability of feedback loop
4. Phase noise and timing jitter

We will first examine the loop filter design to see how it may affect 1 – 3.

Steady State Error. A characteristic of feedback control systems. This is the error remaining in the loop at the comparator output after all transients have died out. In the case of the frequency synthesizer, it is the output from the phase detector, $\phi_{ref} - \phi_{out}$ that constitutes the error, ε.

First we will consider the FS with feedback = 1; therefore, input and output frequencies are identical.



Transfer Function: H(s) = forward path gain / [1 + T(s)].

With feedback = 1,

$$H(s) = T(s)/[1 + T(s)]$$

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_D K_O F(s)/s}{1 + K_D K_O F(s)/s}$$

Phase error function:

$$\varepsilon(s) = \phi_{ref} - \phi_{out} = \frac{s\phi_{ref}}{s + K_D K_O F(s)}$$

For the frequency synthesis application, we want to have ideally perfect phase tracking for phase and frequency steps. When the synthesizer frequency is changed, it is a discontinuous step in modulus, and we want to have zero steady state phase error in this case.

In the phase error analysis for the type 1 passive pole-zero lag filter, we found that there was a static phase error for a frequency step. To eliminate this phase error, we need a TYPE = 2 loop gain function. This requires an ideal integrator rather than a passive lead-lag filter.

Placing an opamp RC integrator or charge pump in the loop will give a filter transfer function of the form:

$$F(s) = \frac{1 + s/\omega_2}{s/\omega_1}$$

where providing a pole at s = 0 and a zero at ω_2. Then, the loop gain T(s) will be that of a type 2 control system:

$$T(s) = \frac{K_D K_O (1 + s/\omega_2)}{s^2/\omega_1}$$

Details regarding the implementation of these filters will be presented later.

Steady State Phase Error

Type 1; second order: $F(s)=\frac{1+s/\omega_2}{1+s/\omega_1}$

Input	$\phi_{ref}(s)$	ε_{ss}
Phase step	$\Delta\theta/s$	0
Freq. step	$\Delta\omega/s^2$	$\Delta\omega/[K_O K_D F(0)]$
Freq. ramp	A/s^3	infinite

Type 2; second order: $F(s)=\frac{1+s/\omega_2}{s/\omega_1}$

Input	$\phi_{ref}(s)$	ε_{ss}
Phase step	$\Delta\theta/s$	0
Freq. step	$\Delta\omega/s^2$	0
Freq. ramp	A/s^3	kA

Now find the closed loop transfer function by inserting F(s).

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_D K_O F(s)/s}{1 + K_D K_O F(s)/s}$$

$$H(s) = \frac{(1 + s/\omega_2)}{\frac{s^2}{K_D K_O \omega_1} + \frac{s}{\omega_2} + 1}$$

Thus, we can see that

$$\omega_n = \sqrt{K_D K_O \omega_1}$$

$$\varsigma = \frac{\omega_n}{2\omega_2}$$

These parameters will have a strong effect on the loop dynamics which control overshoot and settling time. From the system design perspective, overshoot can be quite harmful, since it will cause the frequency to temporarily exceed the steady state value. Thus, the output of the synthesizer might land in an adjacent channel during part of the transient response. Settling time can also be critical since many TDM applications use different receive and transmit frequencies. The settling time determines how long you must wait until transmitting or receiving after a hop in frequency.

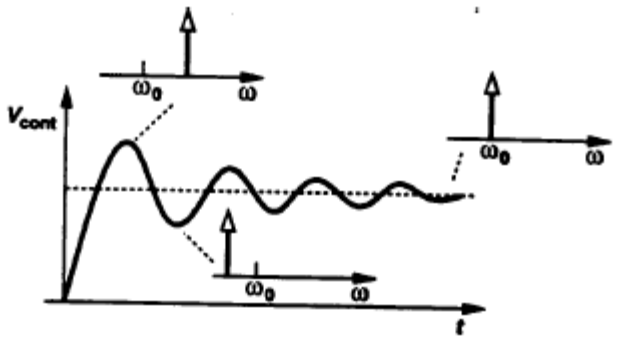


Figure 8.33 Variation of VCO frequency during synthesizer settling.

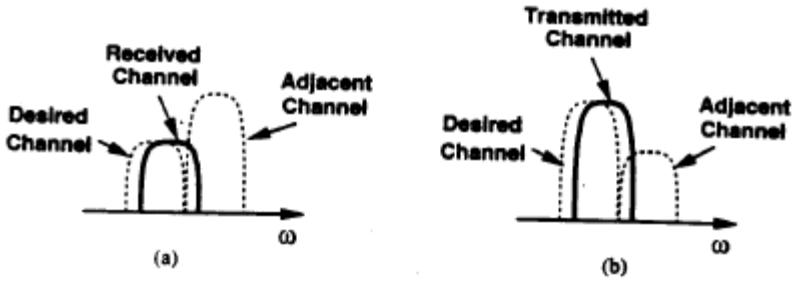


Figure 8.34 Effect of synthesizer settling on received and transmitted channels.

Ref. B. Razavi, RF Microelectronics, Prentice-Hall, 1998.

Here you see the consequences of PLL settling time if the PLL is being used as a local oscillator for a receiver or transmitter.

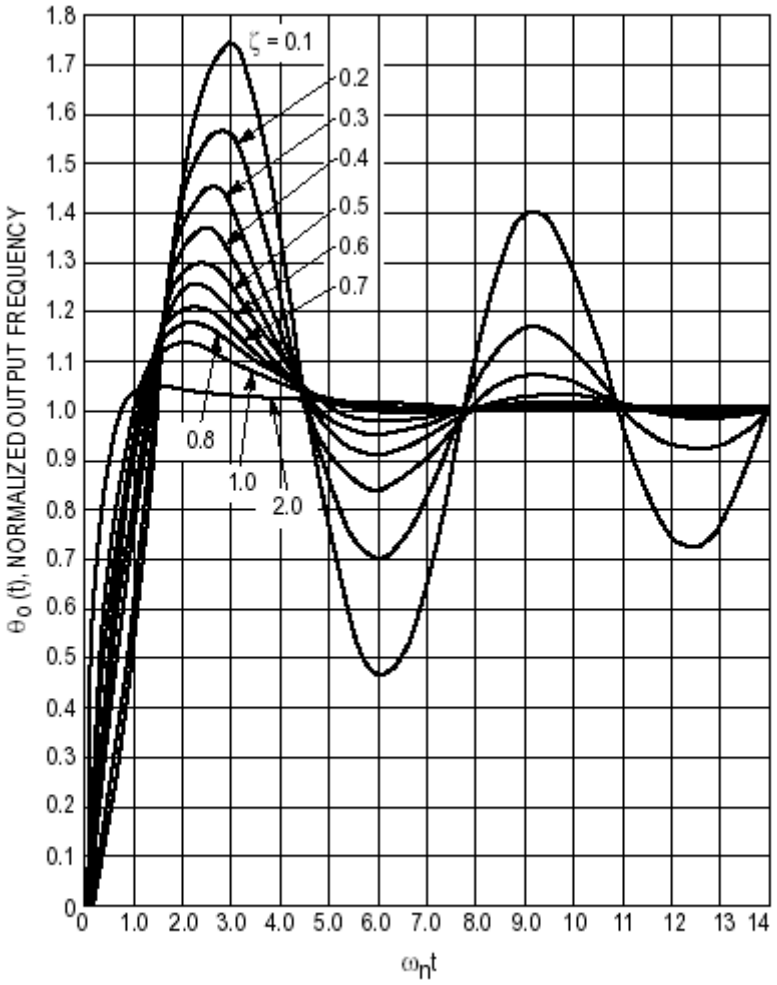


Figure 6. Type 2 Second Order Step Response

Ref. Motorola AN535

Here we see the phase and frequency step response for a type 2 PLL in terms of the key loop parameters. The settling time can be determined by setting an error tolerance around Q = 1. For example, if settling to 5% were the criteria and if $\zeta = 1$, the response first falls within the boundary of 0.95 or 1.05 for $\omega_n t = 4.5$. Then settling time t can be determined since natural frequency ω_n will also be known.

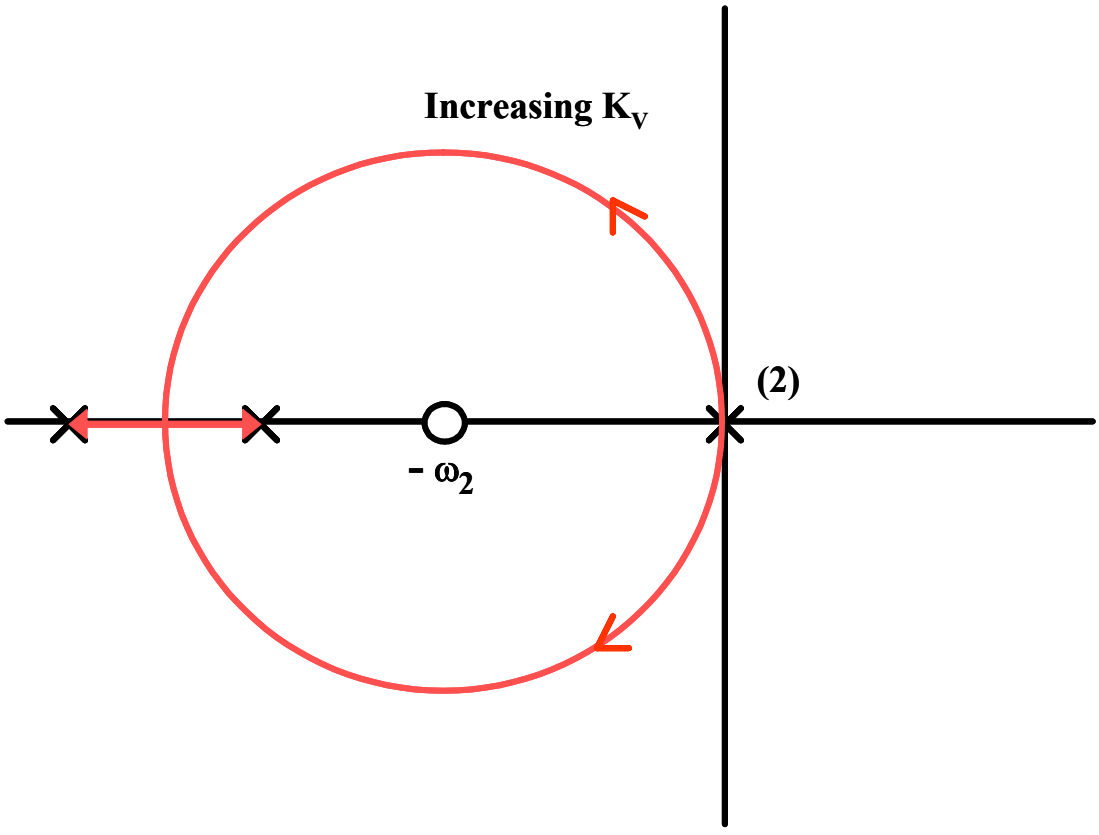
Root Locus:

Now, find the poles of $1 + T(s) = 0$ Let $K_V = K_O K_D$

$$\frac{s^2}{K_V \omega_1} + \frac{s}{\omega_2} + 1 = 0$$

$$s = -\zeta\omega_n \pm \omega_n \sqrt{\zeta^2 - 1}$$

Now examine the root locus. As the loop gain K_V increases, both real and imaginary parts grow. The locus follows a circle centered around the zero. The poles become real again when $\zeta = 1$. This happens when $K_V = 4\omega_2^2/\omega_1$. We have the same geometric interpretation that was discussed in the FMD notes.



Bandwidth: The loop 3 dB bandwidth is important for noise considerations. It is determined by ω_n and ζ, so bandwidth must be determined in conjunction with the overshoot and settling time specifications. We find again that the formula is different for the case with a forward path zero as opposed to the feedback zero case that we discussed in the feedback lectures.

$$\omega_h = \omega_{3dB} = \omega_n \left[1 + 2\zeta^2 + \sqrt{(2\zeta^2 + 1)^2 + 1}\right]^{1/2}$$

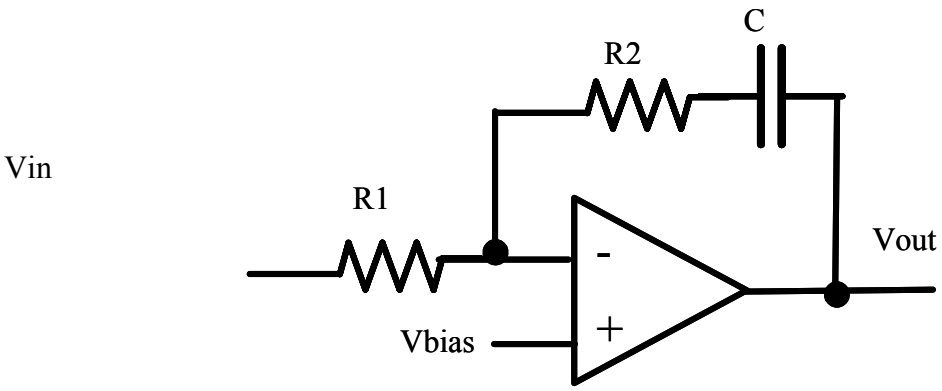
$\omega_{3db} = 2\ \omega_n$ for $\zeta = 0.707$

$\omega_{3db} = 2.5\ \omega_n$ for $\zeta = 1$

Since the loop gain peaking and overshoot is greater when the zero is present, we also expect bandwidth to be higher as this shows.

The effect of bandwidth on the synthesizer noise performance will be discussed later.

Loop Filter – OpAmp



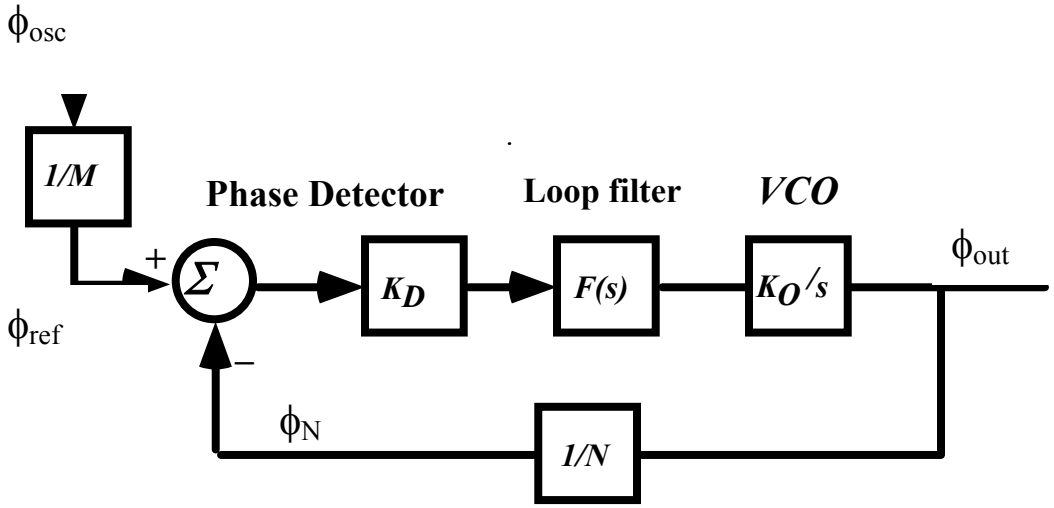
An op amp can be used to form a filter that includes a pole at s = 0 and a finite zero. For example, the circuit above can be analyzed using the virtual ground approximation to obtain F(s).

$$F(s) = \frac{V_{out}}{V_{in}} = \frac{1 + sR_2C}{sR_1C}$$

Vbias can be used to level shift between the phase detector and the VCO.

Synthesizer PLL

We will now add the divider 1/N to the feedback path. This architecture is called an "integer-N" synthesizer.



Thus,

$$\frac{\phi_N}{\phi_{out}} = \frac{1}{N}$$

$$\text{and also, } N = \frac{\omega_{out}}{\omega_{ref}}$$

We can calculate the loop gain, T(s):

$$T(s) = \frac{K_D K_O F(s)}{Ns}$$

- We see that the loop gain is reduced by a factor of N.
- Also, in most applications, N is not constant, so
- $K_V = K_D K_O$ is not a constant – varies with frequency according to the choice of N

Using the F(s) determined for the opamp pole-zero loop filter:

$$F(s) = \frac{1 + s/\omega_2}{s/\omega_1}$$

where $\omega_1 = 1/R_1C$ and $\omega_2 = 1/R_2C$,

$$1 + T(s) = 1 + \frac{K_V}{Ns}\left(\frac{1 + s/\omega_2}{s/\omega_1}\right) = 0$$

$$1 + T(s) = \frac{Ns^2}{K_V\omega_1} + \frac{s}{\omega_2} + 1 = 0$$

We can now determine how the natural frequency and damping are affected by N:

$$\omega_n = \sqrt{\frac{K_V\omega_1}{N}} = \sqrt{\frac{K_V}{R_1CN}}$$

$$\zeta = \frac{\omega_n}{2\omega_2} = \frac{R_2}{2}\sqrt{\frac{K_VC}{R_1N}}$$

Let's design a synthesizer

We can start with a transient specification for locking of the synthesizer PLL

- Overshoot < 20%
- Settling time = 1 mS

From Fig. 6 of AN535 we see that a $\zeta = 0.8$ meets the overshoot spec.

Settling to within 1% happens at $\omega_n t = 5.5$

So, $\omega_n = 5.5/1\text{mS}$

Note that:

1. K_D is fixed. Depends on the phase detector

2. K_O is found from the slope of the VCO tuning curve.
In general, this is not constant, but varies with tuning voltage.

3. N is determined by $\omega_{out}/\omega_{ref}$

The change in N required to tune over the required range and the change in K_O causes the loop gain T to vary with frequency.

Since damping also increases with K_V and decreases with $\sqrt{\frac{1}{N}}$, loop dynamics will depend on N.

4. The phase detector will have a maximum output current.
R_1 must be consistent with V_{DD}/I_{max} Refer to the data sheet.

5. Choose C to determine ω_n

6. Use ζ to determine R_2.

An alternate design sequence could have used the loop bandwidth, $\omega_h = \omega_{3dB}$ as a starting point. We will show later that this is the phase noise corner frequency. From ω_{3dB} and ζ, ω_n could be determined. The settling time is then set by default.

Phase Frequency Detector

The phase-frequency detector shown below is a widely used architecture in frequency synthesizers. As opposed to the XOR phase detector that we first considered, this one produces two outputs: QA and QB, or as is customary, UP and DOWN respectively.

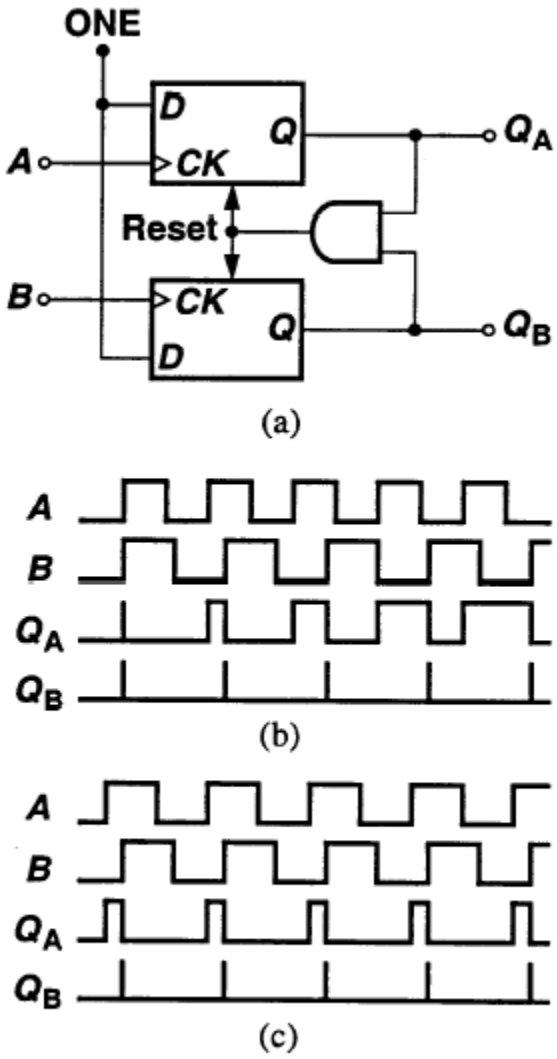
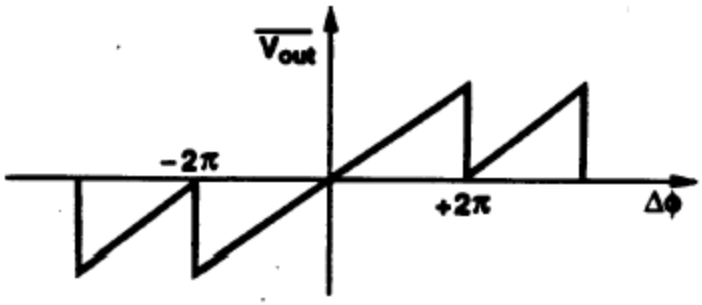


Figure 3.26. (a) Phase/frequency detector. Circuit response with (b) $\omega_A \geq \omega_B$, (A leading B.

Ref. J. Savoj and B. Razavi, High Speed CMOS for Optical Receivers, Kluwer Academic Publishing, 2001. (and many other books)

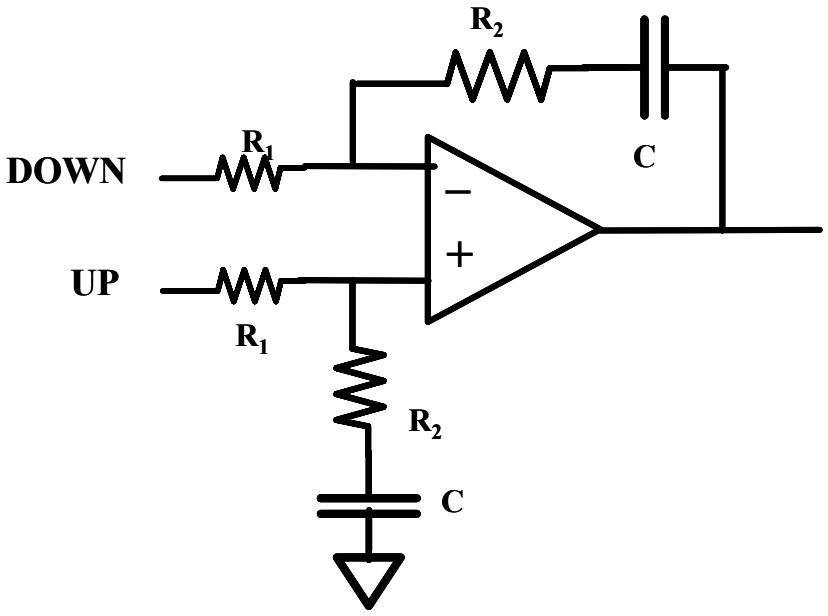
This phase detector has a much larger phase range (4π) of operation, and it will produce an output that drives the frequency in the right direction when it is out of lock. It also has zero offset when the phases are aligned and is insensitive to the duty cycle of the inputs since edge-triggered flip-flops are used.



PFD characteristic.

When the phases coincide, both outputs produce minimum width pulses. When there is a phase or frequency error, the width of the UP or DOWN pulses increases. When integrated by the loop filter, this causes the control voltage of the VCO to move toward the locked condition of equal frequency and phase.

Because both outputs must be combined to obtain the desired output, the loop filter must be modified for differential inputs as shown below. F(s) is the same as that of the single ended version.



Reference Spurs.

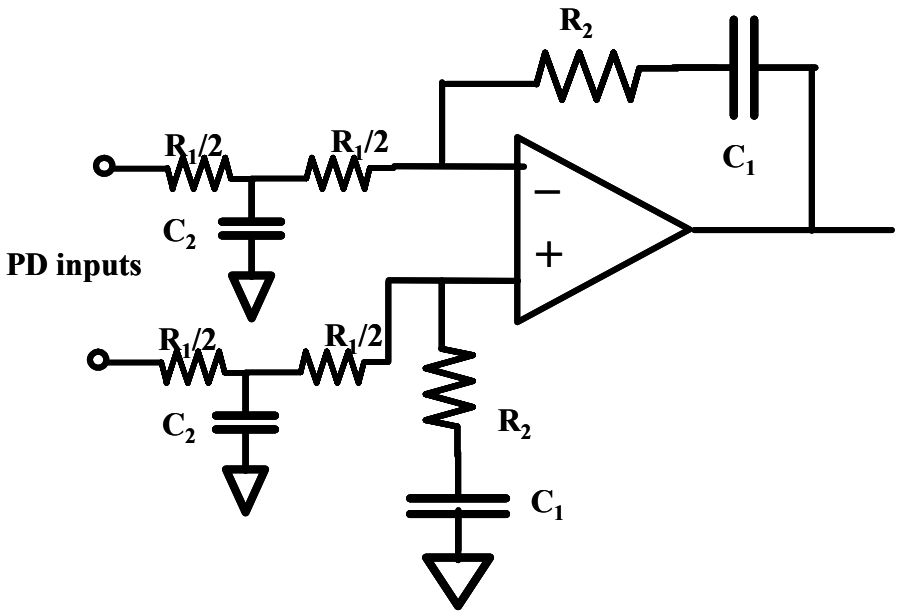
The Integer N PLL has an inherent conflict between the frequency step size (increment) and the settling time/bandwidth. The phase detector produces pulses that are at the reference frequency, f_R. These pulses are filtered by the loop lowpass filter, but not completely. Any residual reference frequency component on the VCO tuning voltage produces frequency modulation. Sidebands called reference spurs appear on both sides of the desired output spectral line spaced by f_R.

The natural frequency of the loop must be well below the reference frequency so that the reference frequency component is well attenuated by the loop filter.

$$\omega_n \leq \omega_R / 10$$

Since the settling time and loop bandwidth are directly affected by ω_n, we have conflicting requirements. Compromises must be made.

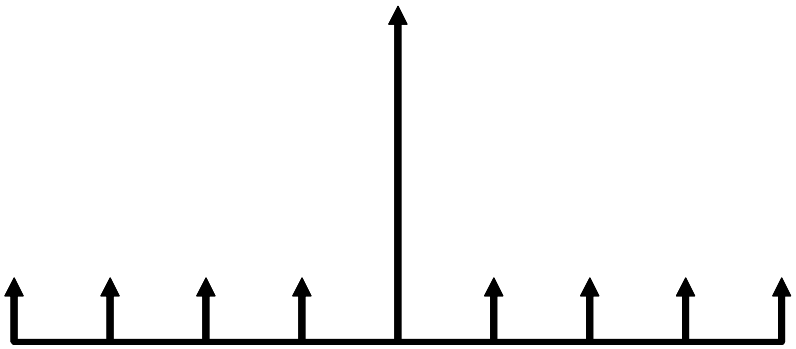
One approach to further reducing reference sidebands is to create a third order loop by adding another pole to the loop filter.



Resistor R1 has been split in half and capacitor C2 added to produce a finite pole at

$$\omega_{C2} = 4 / R_1 C_2 .$$

This suppresses the reference spurs by a factor of ω_R/ω_{C2} at the expense of stability. This restriction will be discussed further in the charge pump loop filter section below.



Reference sidebands (spurs)

Charge Pump Loop Filter

An alternative loop filter implementation called the charge pump is widely used for many applications. It is very convenient to implement in CMOS.

- The PFD output produces UP (Q_A) and DOWN (Q_B) pulses whose width is proportional to the phase error.

- Charge pump current sources I_1 and I_2 must produce exactly equal currents. They charge and discharge the capacitor, C_P, in discrete steps.

- If there is a static phase error $\Delta\phi$ at the PFD input, the capacitor, C, will be charged indefinitely – therefore, the DC gain is infinite: an ideal integrator. So, we expect to have zero static phase error. This is unlike the type I loop which gave $\Delta\phi = \Delta\omega/K_V$ steady state phase error.

- The CP PLL will detect small phase errors and correct them as long as the frequency of the phase error (jitter frequency) is within the loop 3 dB bandwidth. This phase comparison occurs on every cycle.

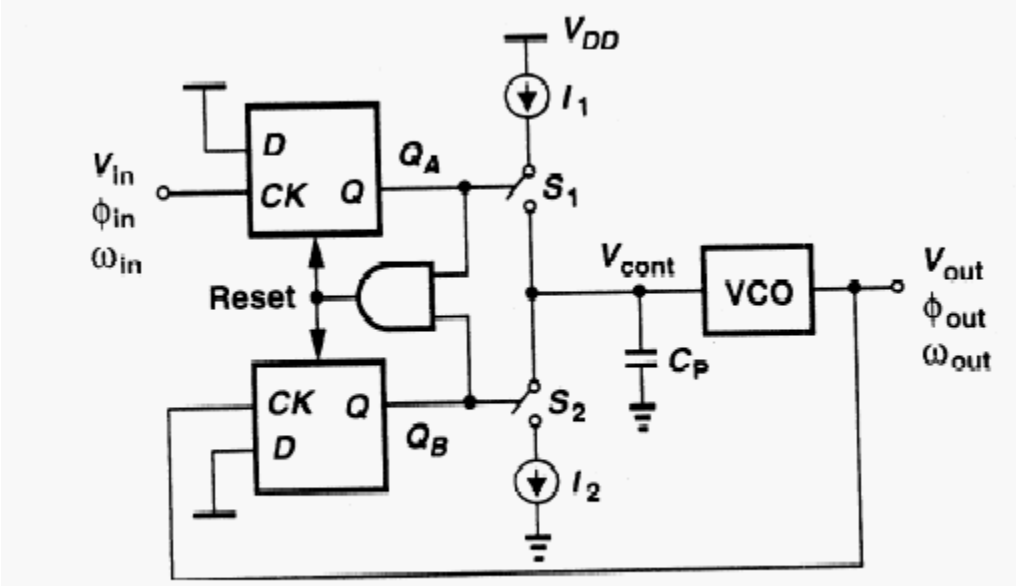


Figure 15.30 Simple charge-pump PLL.

(from B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.

To illustrate how the charge pump works and how it might be analyzed in a linearized model, refer to Fig. 15.32. Here we assume that $I_1 = I_2 = I_P$ and that a phase step $\Delta\phi$ occurs at t = 0.

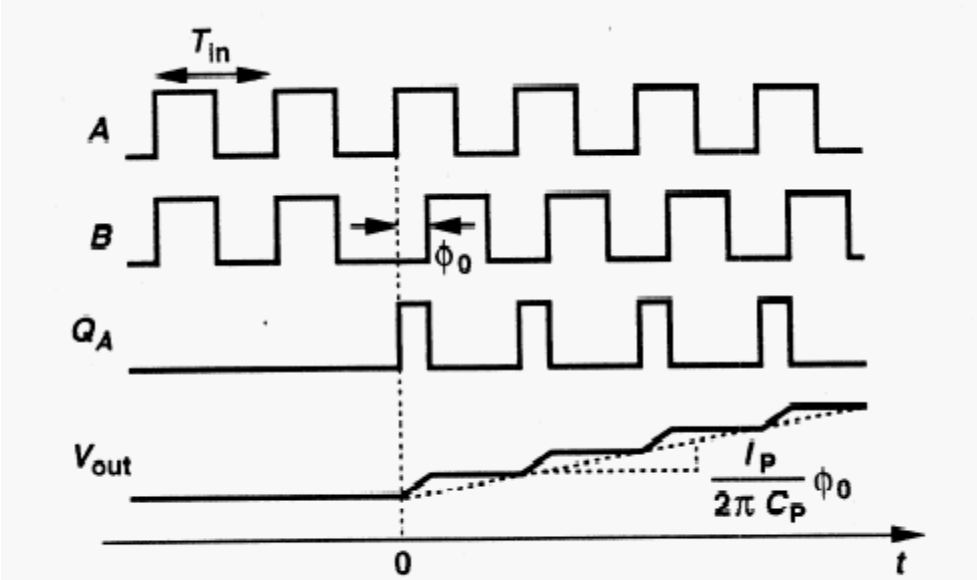


Figure 15.32 Step response of PFD/CP/LPF combination.

(from B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.

First consider the time domain picture above. $\Delta\phi = \phi_0\, u(t)$

Q_A produces pulses that are of width

$$\frac{\Delta\phi}{2\pi} T_{in} = \Delta t \ .$$

I_P charges Cp by

$$\Delta V = \frac{I_P}{C_P}\Delta t = \frac{I_P}{C_P}\frac{\phi_0}{2\pi} T_{in}$$

in every period. We can approximate this as a linear ramp with slope

$$slope = \frac{I_P}{2\pi C_P}\phi_0$$

Thus, the output voltage from the charge pump can be described by

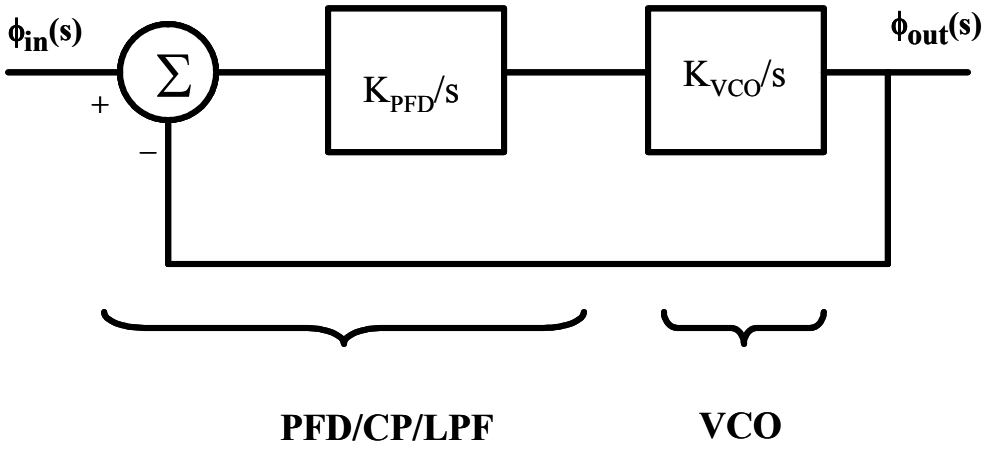
$$V_{out}(t) = \frac{I_P \phi_0}{2\pi C_P} t\, u(t)$$

The derivative of the step response is the impulse response, so we can determine the frequency domain transfer function.

$$h(t) = \frac{dV_{out}}{dt} = \frac{I_P}{2\pi C_P} u(t)$$

Take the Laplace transform to obtain the frequency domain transfer function.

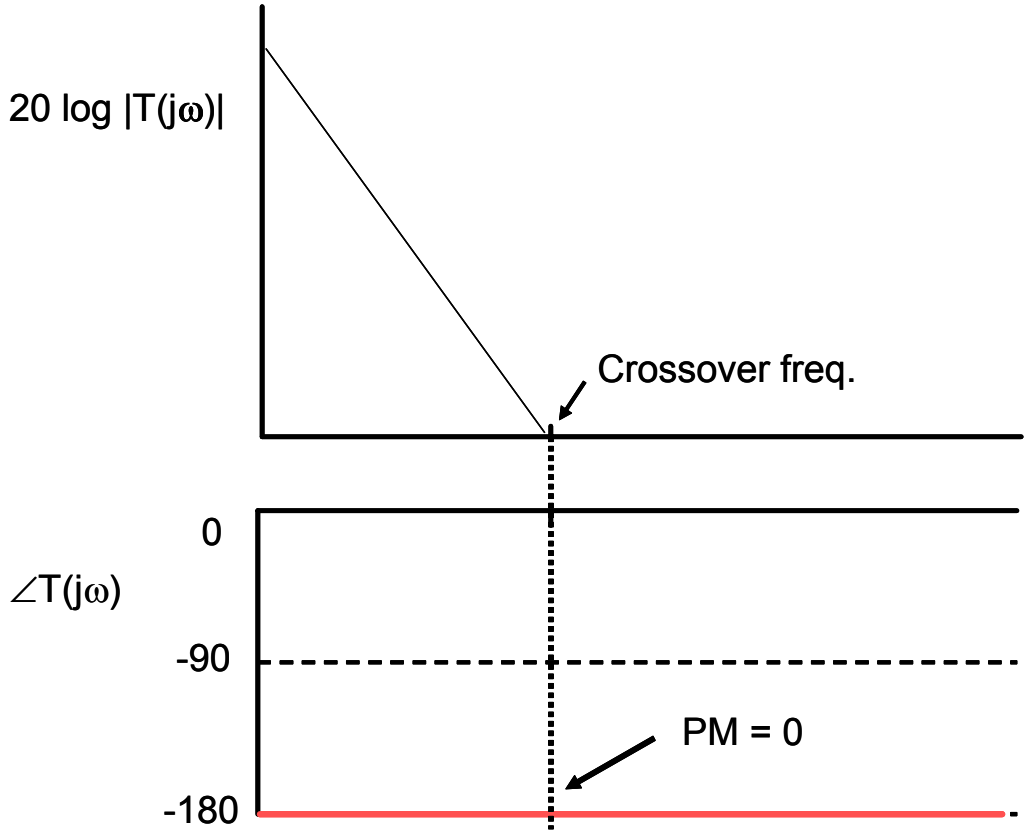
$$H(s) = \frac{V_{out}(s)}{\Delta\phi} = \frac{I_P}{2\pi C_P} \frac{1}{s} = \frac{K_{PFD}}{s}$$



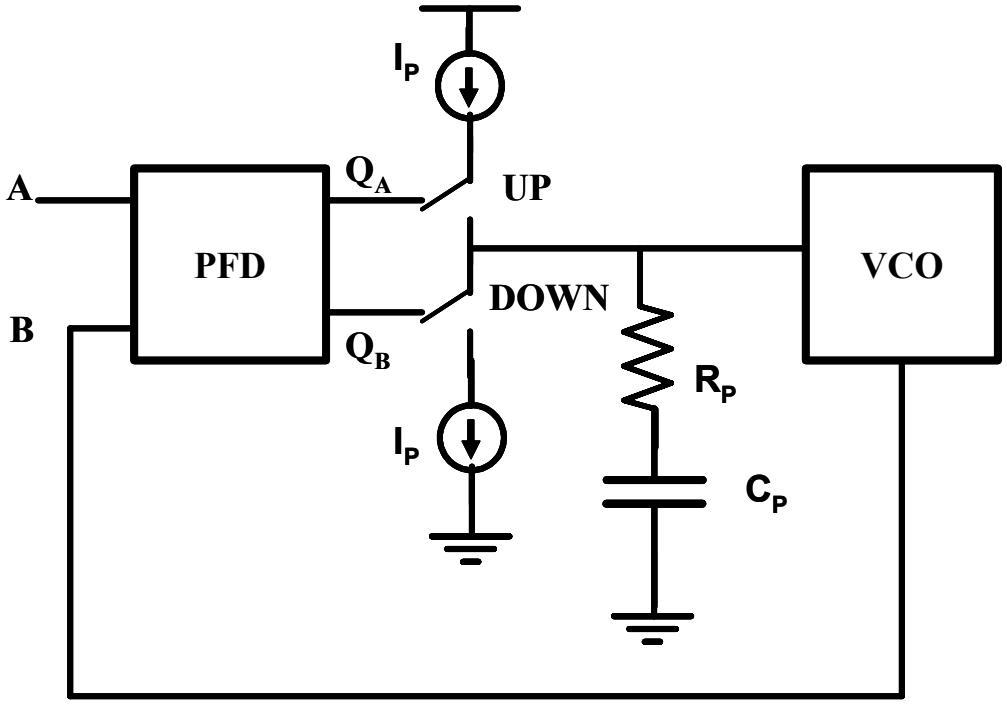
Here is the block diagram of the CP PLL. We see that the loop gain function T(s) has a factor of s^2 in the denominator. Thus, it is a type II loop.

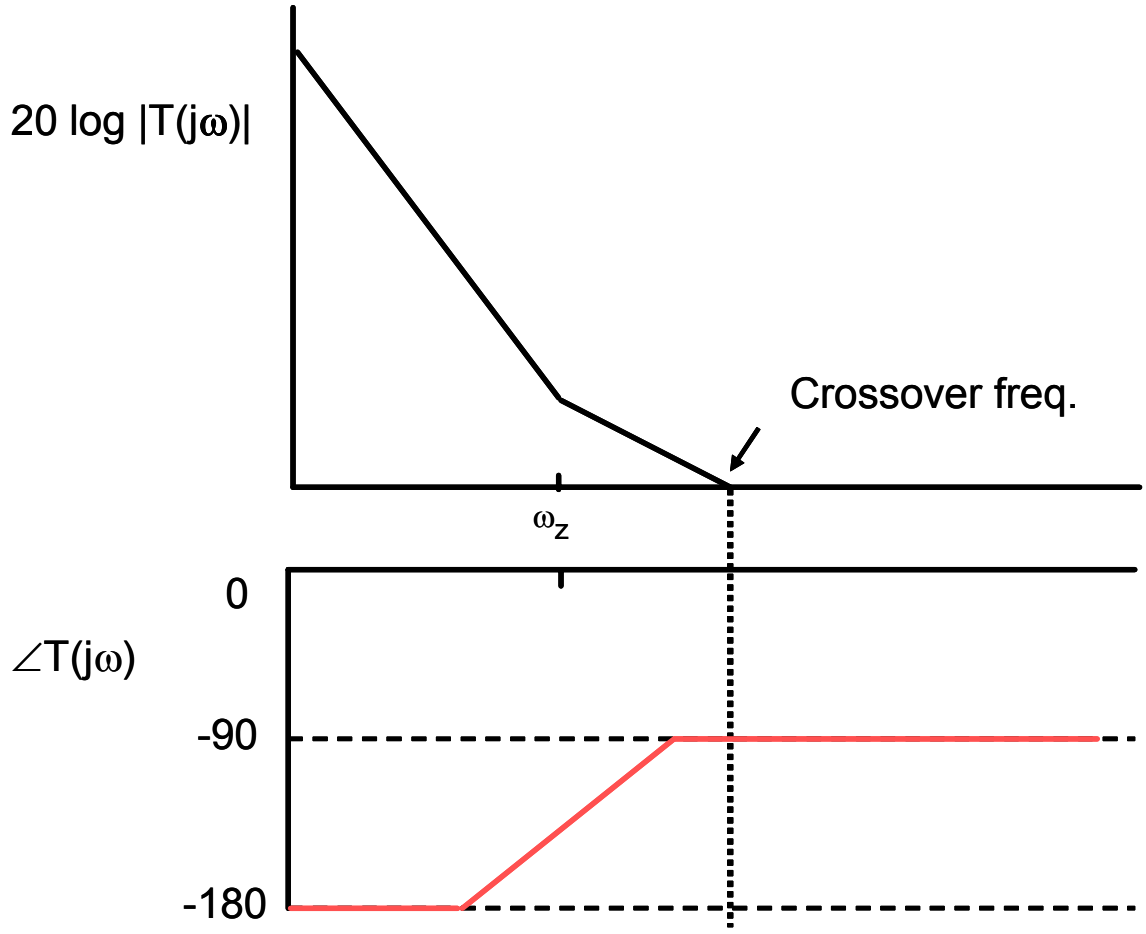
$$T(s) = \frac{K_{PFD}}{s} \frac{K_{VCO}}{s}$$

But, because of that, we have a big problem. The phase margin is always zero as shown by the Bode plot below.



Therefore, we must add a zero to the loop filter transfer function to provide some phase lead to stabilize the PLL.

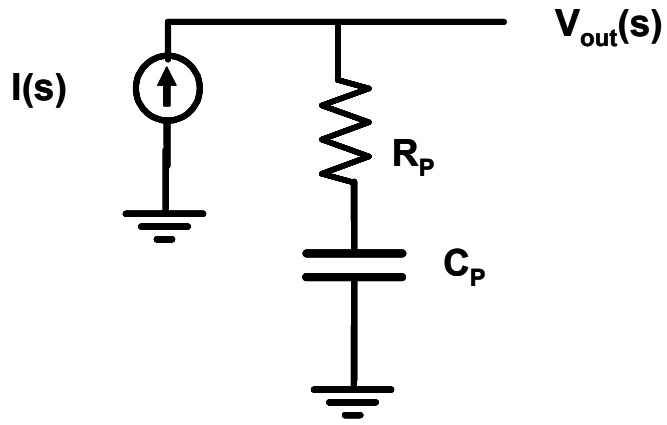




Now, we can see that an increase in the loop gain will improve phase margin.

To determine T(s) for this case, we want to calculate Vout(s)/Δϕ again, adding the resistor to the charge pump filter.

New filter:



The phase frequency detector (PFD) with single capacitor C_P has

$$H(s) = \frac{V_{out}(s)}{\Delta\phi} = \frac{I_P}{2\pi C_P}\frac{1}{s} = \frac{K_{PFD}}{s}$$

To find the frequency response of the input current, we note that,

$$I(s) = Vout(s)/Z(s) = Vout(s)/(1/sC_P)$$

where Z(s) is the complex impedance. So, the current source can be modeled as:

$$\frac{I(s)}{\Delta\phi} = \frac{I_P}{2\pi} \quad .$$

Now, let's use this to modify H(s) for the series RC loop filter. To do this, just replace the impedance $1/sC_P$ with $Z(s) = R_P + 1/sC_P$.

$$\frac{Vout(s)}{\Delta\phi} = \frac{I_P}{2\pi}\left(R_P + \frac{1}{sC_P}\right).$$

The loop gain T(s) is therefore

$$T(s) = \frac{\phi_{out}(s)}{\phi_{in}} = \frac{I_P}{2\pi}\left(R_P + \frac{1}{sC_P}\right)\frac{K_{VCO}}{s}$$

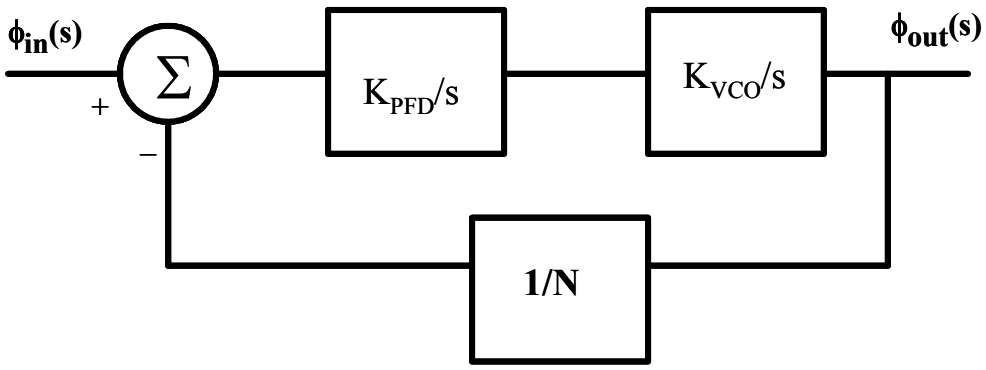
$$= \frac{I_P K_{VCO}}{2\pi C_P}\,\frac{\left(R_P C_P s + 1\right)}{s^2}$$

We see that a zero at $\omega = 1/R_PC_P$ has been added to the transfer function. This provides the necessary phase lead to achieve stability.

Of course a frequency divider can be placed in the feedback path if the output frequency is to be multiplied by the PLL. Divide by N gives

$$\phi_{out} = N\phi_{in}$$
$$\omega_{out} = N\omega_{in}$$

This added divider would be needed in a frequency synthesizer application or clock multiplier application.



T(s) is then modified by a factor of 1/N.

$$T(s) = \frac{I_P K_{VCO}}{2\pi N C_P} \frac{(R_P C_P s + 1)}{s^2}$$

Now, let's retain the factor of 1/N for completeness, and derive the closed loop transfer function. Define $K_V = I_P K_{VCO}/2\pi C_P$ and zero frequency $w_Z = 1/R_P C_P$.

$$\frac{\phi_{out}(s)}{\phi_{in}} = \frac{K_V (s/\omega_z + 1)/s^2}{1 + K_V (s/\omega_z + 1)/Ns^2}$$

$$= \frac{N(s/\omega_z + 1)}{\frac{N}{K_V} s^2 + \frac{s}{\omega_z} + 1}$$

Having put this in one of the standard forms, we can extract ω_n and ζ from the denominator.

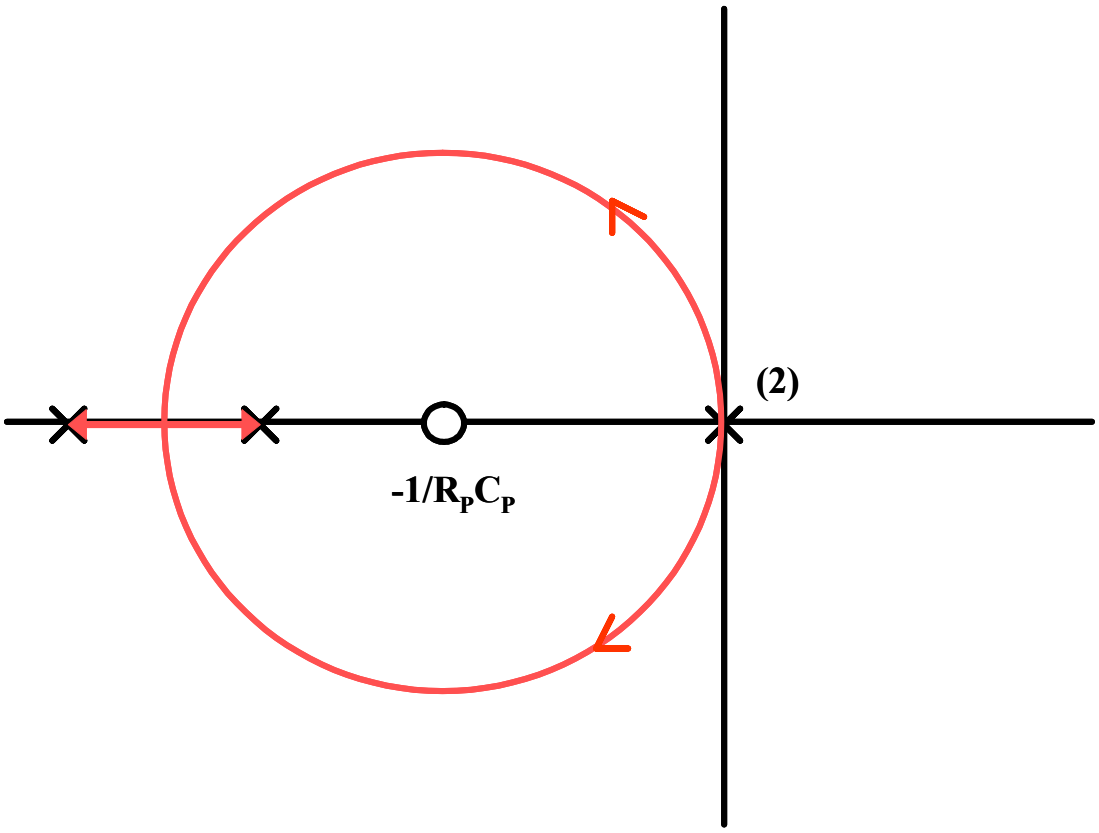
$$\omega_n = \sqrt{\frac{K_V}{N}} = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P N}}$$

$$\zeta = \frac{\omega_n}{2\omega_z} = \frac{R_P}{2}\sqrt{\frac{I_P K_{VCO} C_P}{2\pi N}}$$

We can see now with $R_P = 0$, $\zeta = 0$, therefore there is no phase margin and the system is unstable as expected. With added R_P, the damping factor can be increased. Also note

that stability will decrease with increasing N. Loop gain must be increased to compensate for this.

The root locus of the modified charge pump PLL is shown below. It is the same as was obtained for the opamp loop filter.



As loop gain is increased by increasing $I_P K_{VCO}$, the dual poles at s = 0 split and form a circular locus, rejoining the real axis at $-1/2R_PC_P$.

The pole locations are found at

$$s = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$$

Closed Loop Frequency Response

The closed loop frequency response can be evaluated from H(jω). In Fig. 2-3, Gardner has plotted the magnitude as a function of ω/ω_n.

Bandwidth: The loop 3 dB bandwidth is important for noise considerations. It is determined by ω_n and ζ, so bandwidth must be determined in conjunction with the overshoot and settling time specifications. We find again that the formula is different for the case with a forward path zero as opposed to the feedback zero case that we discussed in the feedback lectures.

$$\omega_h = \omega_{3dB} = \omega_n \left[1 + 2\zeta^2 + \sqrt{(2\zeta^2 + 1)^2 + 1}\right]^{1/2}$$

$\omega_{3db} = 2\ \omega_n$ for $\zeta = 0.707$

$\omega_{3db} = 2.5\ \omega_n$ for $\zeta = 1$

Since the loop gain peaking and overshoot is greater when the zero is present, we also expect bandwidth to be higher as this shows.

We see that the frequency response is a low pass to ϕin. Thus, the phase noise of the reference source passes through the PLL and is filtered as shown in Fig. 2-3. Below the 3 dB frequency, we have little attenuation of input noise. Above, noise is reduced by 40 dB/decade.

Also note that for $\zeta < 2$, there is gain peaking. Actually there is always some gain peaking for the Type II CP PLL or the opamp filter PLL because the zero frequency is always less than the pole frequency in the strongly damped case. For some applications, this is inconsequential. However, for clock and data recovery (CDR) use, the SONET specification is very strict: less than 0.1 dB of gain peaking is allowed. This is because in an optical fiber link, the signal may pass through several repeaters that include CDR units. Cascaded transfer functions with gain peaking leads to amplification of jitter (phase noise) close to the 3 dB frequency.

F.M. Gardner, Phaselock Techniques, Wiley 1979.

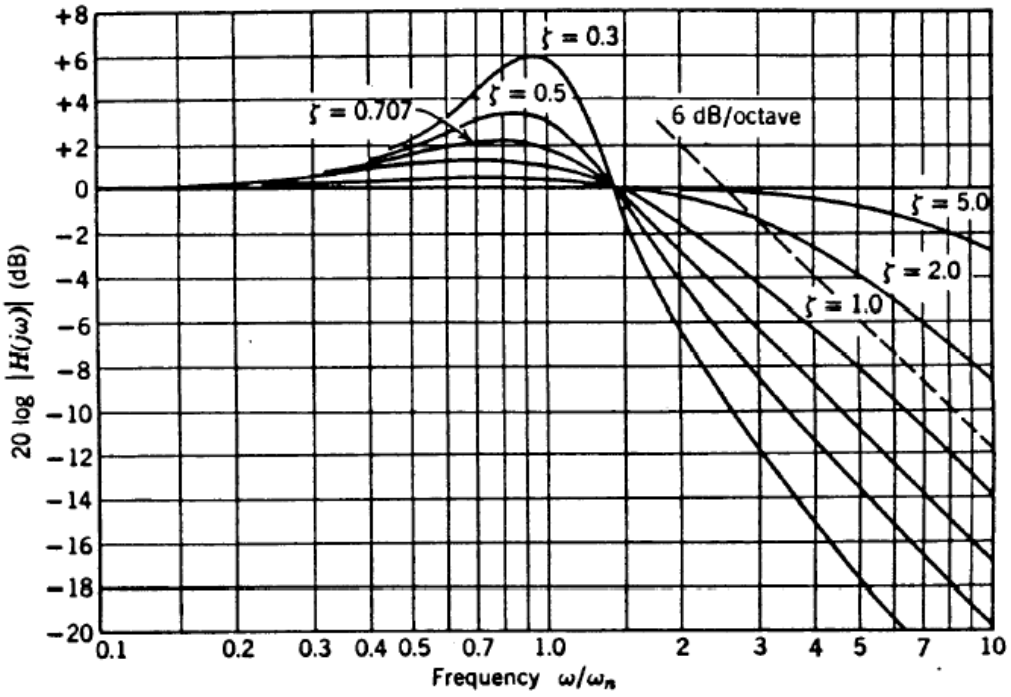


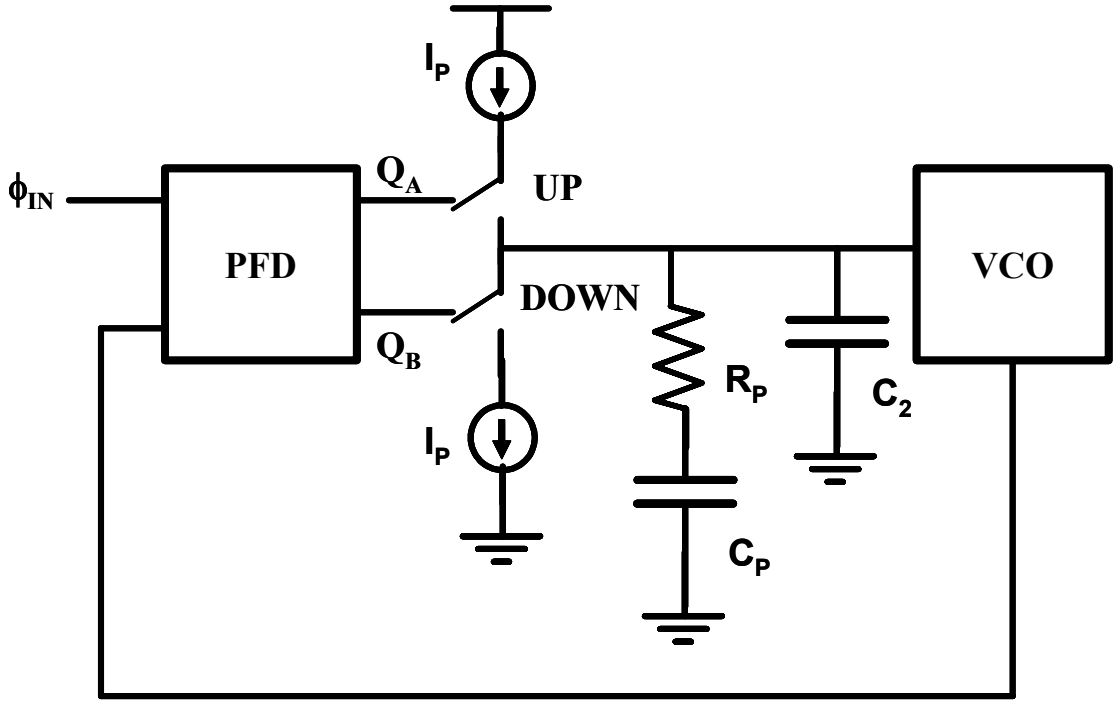
Figure 2.3 Frequency response of a high-gain second-order loop.

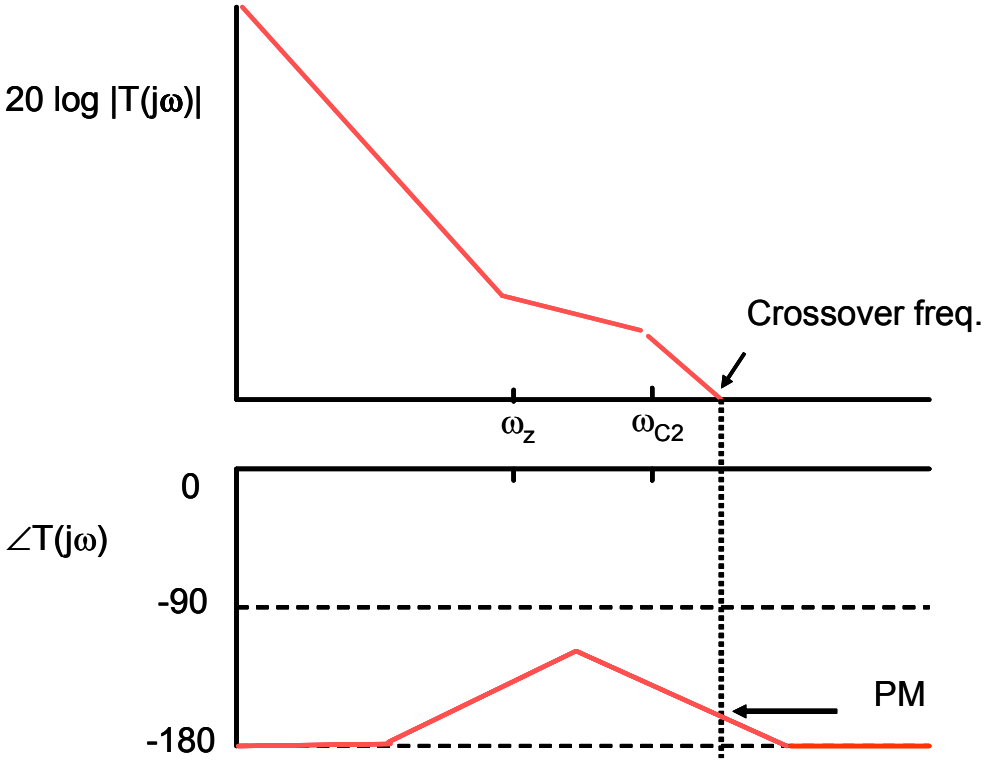
Third-order CP PLL

There is still one residual problem that we have overlooked. The phase detector produces pulses of variable width that activate the switches to either charge or discharge the capacitor C_P. Now that we have added the resistor, however, we find that the control voltage coming out of the charge pump will jump up or down before settling to its steady state value. This occurs because you cannot change the voltage across a capacitor instantaneously, so the initial voltage drop occurs across R_P, which then charges C_P exponentially. This jumpy control voltage frequency modulates the VCO at the reference frequency, creating reference spurs. This is not such a big problem if N = 1 because the jump will be at the same frequency as the VCO. But, at larger N values, it creates sidebands and jitter.

So, we need to fix this by adding a second capacitor, C_2, whose function is to filter out the jumpy response of the series RC network. The magnitude of the reference spur sidebands is reduced by a factor of ω_{REF}/ω_{C2}. Unfortunately, however, C_2 adds a third

pole of finite frequency that will reduce the stability of the PLL. A look at the Bode plot verifies this. $\omega_{C2} = \dfrac{C_P + C_2}{R_P C_P C_2}$





The pole frequency is given by R_P in parallel with the series combination of C_P and C_2. Thus, the pole is always higher in frequency than the zero. We can see that the added pole reduces the phase margin. In fact, now when the loop gain is increased, phase margin is reduced. So, we must be careful that the pole frequency added by C_2 is much higher than the loop bandwidth.

$$\omega_{C2} >> 10\ \omega_N$$

For any C_P/C_2 ratio, it can be shown that the maximum phase margin is [1]

$$PM_{max} = 2\tan^{-1}\left(\sqrt{C_P/C_2 + 1}\right) - \frac{\pi}{2}\ .$$

and the new crossover frequency can be estimated from

$$\omega_x = \sqrt{\frac{C_P/C_2 + 1}{C_P R_P}}$$

- The phase margin equation leads to a guideline that $C_P > 20C_2$ in order to obtain a minimum of 65 degree phase margin (corresponds to $\zeta = 0.707$). Many applications will require larger damping than this. In this regime, the analysis can be considered an extension of the second order PLL analysis. Use the open loop analysis to estimate the required loop gain and corresponding phase margin.

- In addition, ω_N should be no larger than $\omega_{REF}/10$ so that the continuous time approximation is valid.

[1] A. Chandrakasan, W. Bowhill, F. Fox, *Design of High Performance Microprocessor Circuits*, Chap. 12, IEEE Press, 2001.

PLL Phase Noise

We have considered how the bandwidth of the loop affects things like settling time and capture range. But it also plays a role in the PLL noise behavior.

For frequency synthesis, we are interested in low phase noise. There are at least 2 main sources:

1. reference noise – usually small since we frequently use a crystal oscillator

2. VCO noise – often high. We hope that the PLL will suppress most of the noise, at least close to the carrier.

The effect caused by each of these noise sources can be seen from the closed loop transfer functions.

Phase noise filtering by the PLL:

Reference Noise:

$$\frac{\phi_{out}}{\phi_{ref}} = \frac{Forward\ Path}{1+T(s)} = \frac{K_V F(s)/s}{1+K_V F(s)/Ns}$$

$$= \frac{N(1+s/\omega_2)}{Ns^2/K_V + s/\omega_2 + 1}$$

This is a low pass transfer function. Its magnitude approaches N as s becomes small. Thus, reference phase noise is low pass filtered by the loop. Reference phase noise can be quite low when a crystal oscillator is used to generate the reference frequency. However, the phase noise gets multiplied by a factor of N for the integer N PLL.

$$\frac{\phi_{out}}{\phi ref} = N$$

This is a serious limitation for large N values. There are better architectures to be used when small step size and low phase noise are both required.

VCO Noise:

$$\frac{\phi_{out}}{\phi_{vco}} = \frac{Forward\ Path}{1+T(s)} = \frac{1}{1+K_V F(s)/Ns}$$

$$= \frac{Ns^2/K_V}{Ns^2/K_V + s/\omega_2 + 1}$$

This is a high pass closed loop transfer function. It approaches a magnitude of 1 as s becomes large.

While LC VCOs can have low phase noise, they generally have smaller tuning range. RC or ring oscillator VCOs can be built with very wide tuning range but poor phase noise. The PLL can be used to clean up the VCO phase noise within the loop bandwidth. VCO phase noise is unattenuated at offset frequencies beyond the loop bandwidth.

Conclusions:

1. Reference input noise (reference source noise, data jitter, phase noise on FM input signal, etc.) sees a low-pass transfer function. It is passed through and multiplied by N. All we can do is try to avoid making it worse with our loop. A narrow bandwidth loop filter will help to suppress high frequency noise coming into the PLL from the reference port.

2. VCO jitter is suppressed by the PLL within the loop bandwidth. It has a high-pass transfer function. Thus, to suppress VCO noise, we want a large loop bandwidth.