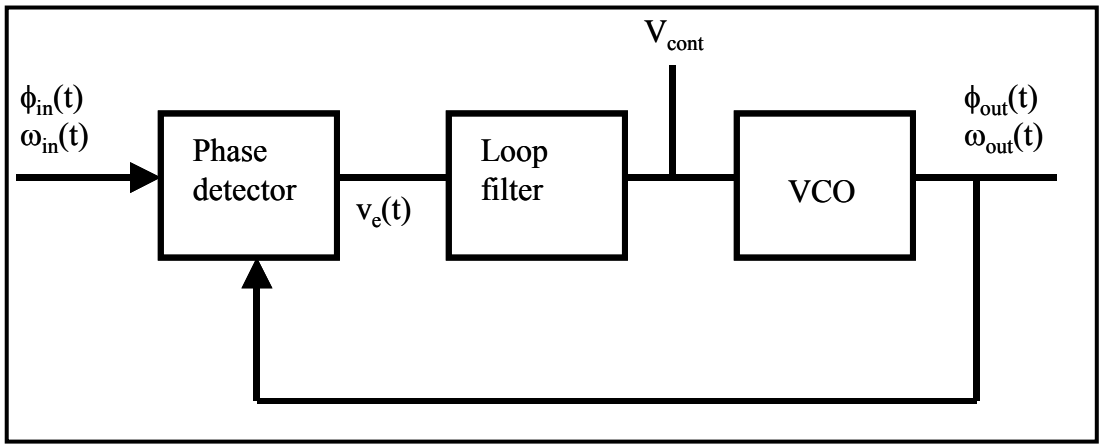
Phase Locked Loop Circuits
ECE145B/ECE218B

Reading: General PLL Description: T. H. Lee, Chap. 15. Gray and Meyer, 10.4
Clock generation: B. Razavi, *Design of Analog CMOS Integrated Circuits*, Chap. 15, McGraw-Hill, 2001.

1. **Definition.** A PLL is a feedback system that includes a VCO, phase detector, and low pass filter within its loop. Its purpose is to force the VCO to replicate and track the frequency and phase at the input when in lock. The PLL is a control system allowing one oscillator to track with another. It is possible to have a phase offset between input and output, but when locked, the frequencies must exactly track.

$$\phi_{out}(t) = \phi_{in}(t) + const.$$
$$\omega_{out}(t) = \omega_{in}(t)$$

The PLL output can be taken from either V_{cont}, the filtered (almost DC) VCO control voltage, or from the output of the VCO depending on the application. The former provides a baseband output that tracks the phase variation at the input. TheVCO output can be used as a local oscillator or to generate a clock signal for a digital system. Either phase or frequency can be used as the input or output variables.



Of course, phase and frequency are interrelated by:

$$\omega(t) = \frac{d\phi}{dt}$$

$$\phi(t) = \phi(0) + \int_0^t \omega(t')dt'$$

Applications: There are many applications for the PLL, but we will study three:

a. FM demodulator
b. Frequency synthesizer
c. Clock generation

You should note that there will be different input and output variables and different design criteria for each case, but you can still use the same basic loop topology and analysis methods.

2. Phase detector: compares the phase at each input and generates an error signal, $v_e(t)$, proportional to the phase difference between the two inputs. K_D is the gain of the phase detector (V/rad).

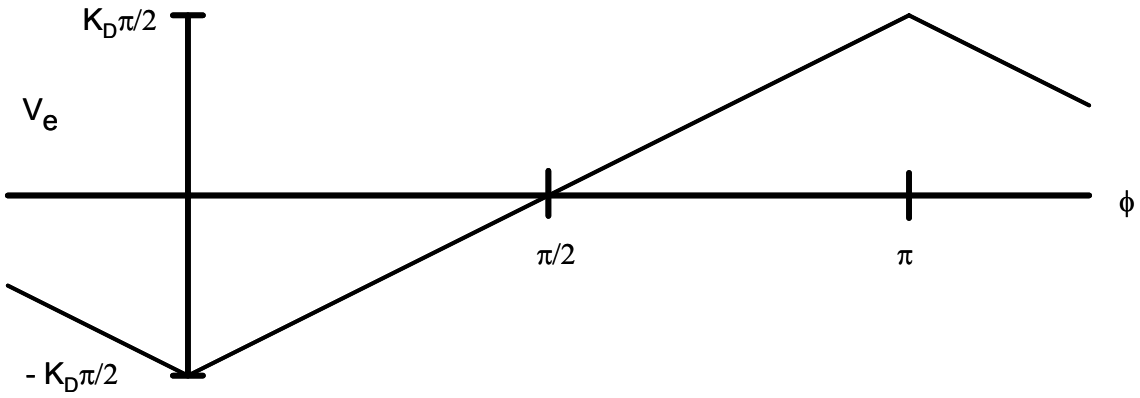
$$v_e(t) = K_D[\phi_{out}(t) - \phi_{in}(t)]$$

As one familiar circuit example, an analog multiplier or mixer can be used as a phase detector. Recall that the mixer takes the product of two inputs. $v_e(t) = A(t)B(t)$. If,

$$A(t) = A\cos(\omega_0 t + \phi_A)$$
$$B(t) = B\cos(\omega_0 t + \phi_B)$$
$$\text{Then, } A(t)B(t) = (AB/2)[\cos(2\omega_0 t + \phi_A + \phi_B) + \cos(\phi_A - \phi_B)]$$

Since the two inputs are at the same frequency when the loop is locked, we have one output at twice the input frequency and an output proportional to the cosine of the phase difference. The doubled frequency component must be removed by the lowpass loop filter. Any phase difference then shows up as the control voltage to the VCO, a DC or slowly varying AC signal after filtering.

The averaged transfer characteristic of such a phase detector is shown below. Note that in many implementations, the characteristic may be shifted up in voltage (single supply/single ended).



If the phase difference is $\pi/2$, then the average or integrated output from the XOR-type phase detector will be zero (or VDD/2 for single supply, digital XOR). The slope of the characteristic in either case is K_D.

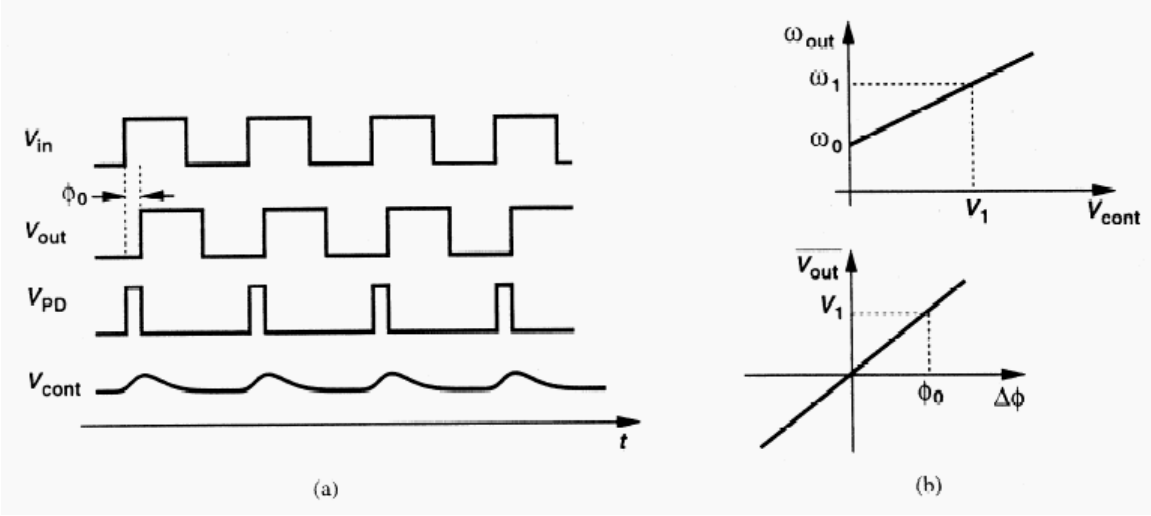
3. VCO. In PLL applications, the VCO is treated as a linear, time-invariant system. Excess phase of the VCO is the system output.

$$\phi_{out} = K_O \int_{-\infty}^{t} V_{cont}\, dt'$$

The VCO oscillates at an angular frequency, ω_{out}. Its frequency is set to a nominal ω_0 when the control voltage is zero. Frequency is assumed to be linearly proportional to the control voltage with a gain coefficient K_O or K_{VCO} (rad/s/v).

$$\omega_{out} = \omega_0 + K_O V_{cont}$$

Thus, to obtain an arbitrary output frequency (within the VCO tuning range, of course), a finite V_{cont} is required. Let's define $\phi_{out} - \phi_{in} = \Delta\phi$.



(Figure from B. Razavi, Ch. 15, op. cit.)

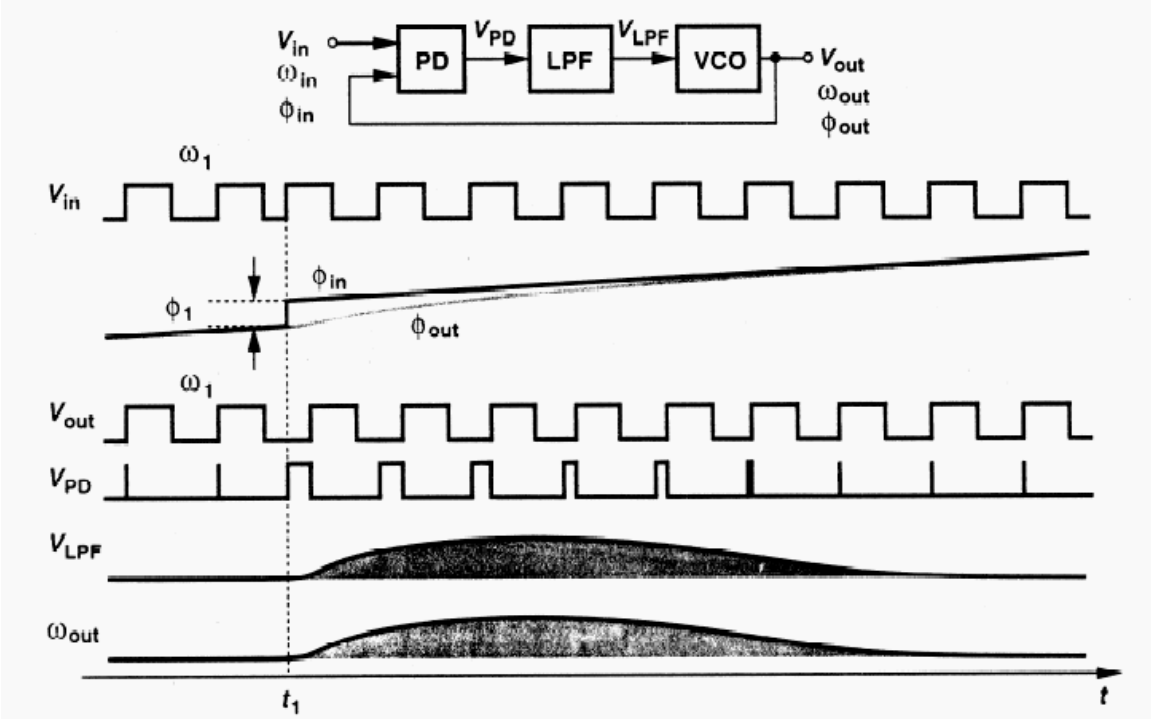
In the figure above, the two inputs to the phase detector are depicted as square waves. The XOR function produces an output pulse whenever there is a phase misalignment. Suppose that an output frequency ω_1 is needed. From the upper right figure, we see that a control voltage V_1 will be necessary to produce this output frequency. The phase detector can produce this V_1 only by maintaining a phase offset ϕ_0 at its input. In order to minimize the required phase offset or error, the PLL loop gain, $K_D K_O$, should be maximized, since

$$\phi_0 = \frac{V_1}{K_D} = \frac{\omega_1 - \omega_0}{K_D K_O}$$

Thus, a high loop gain is beneficial for reducing phase errors.

4. PLL dynamic response: To see how the PLL works, suppose that we introduce a phase step at the input at $t = t_1$.

$$\phi_{in} = \omega_1 t + \phi_0 + \phi_1 u(t - t_1)$$



(Figure from B. Razavi, Ch. 15, op. cit.)

Since we have a step in phase, it is clear that the initial and final frequencies must be identical: ω_1. But, a temporary change in frequency is necessary to shift the phase by f1. The area under ω_{out} gives the additional phase because Vcont is proportional to frequency.

$$\phi_1 = \int_{t_1}^{\infty} \omega_{out}\, dt = \int_{t_1}^{\infty} K_O V_{cont}(t) dt$$

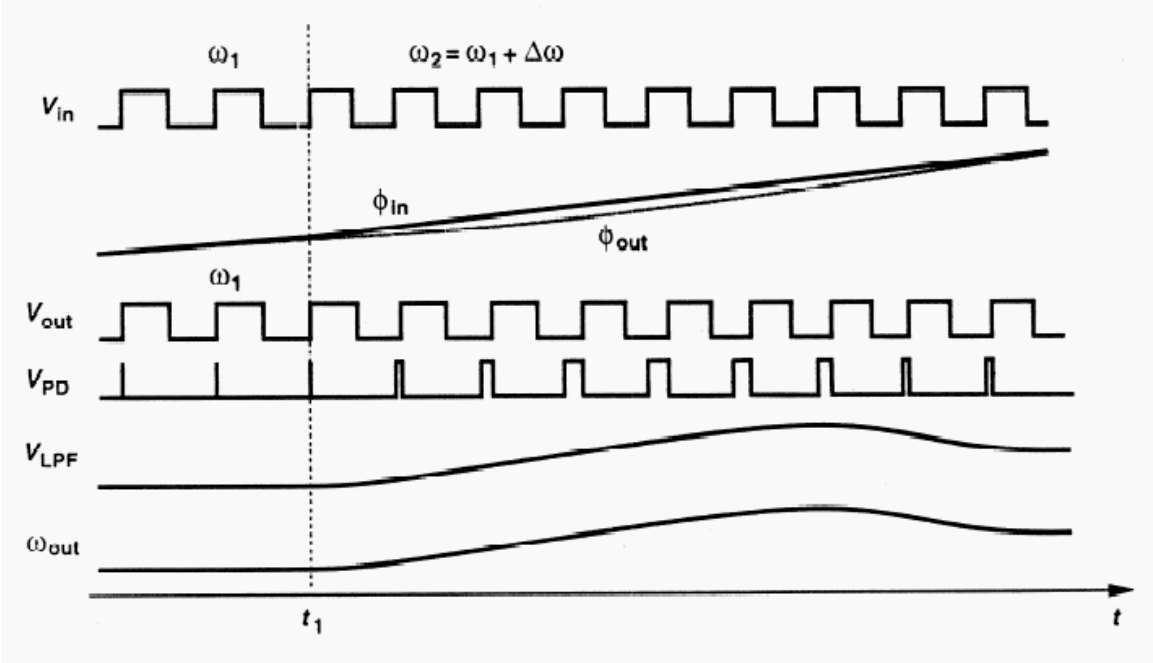
After settling, all parameters are as before since the initial and final frequencies are the same. This shows that Vcont (t) can be used to monitor the dynamic phase response of the PLL.

Now, let's investigate the behavior during a frequency step:

$$\omega_2 = \omega_1 + \Delta\omega$$

The frequency step will cause the phase difference to grow with time since a frequency step is a phase ramp. This in turn causes the control voltage, V_{cont}, to increase, moving

the VCO frequency up to catch up with the input reference signal. In this case, we have a permanent change in ω_{out} since a higher V_{cont} is required to sustain a higher ω_{out}.

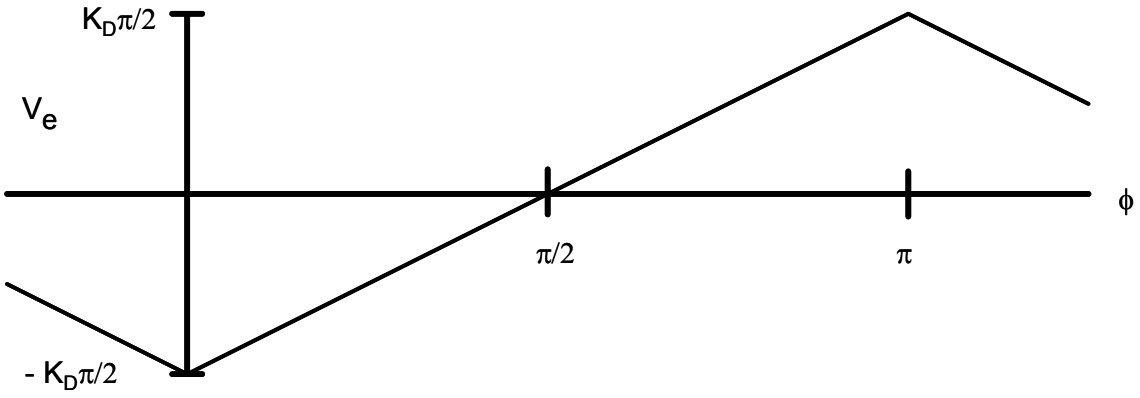


(Figure from B. Razavi, Ch. 15, op. cit.)

If the frequency step is too large, the PLL will lose lock.

5. Lock Range. Range of input signal frequencies over which the loop remains locked once it has captured the input signal. This can be limited either by the phase detector or the VCO frequency range.

a. If limited by phase detector:



$0 < \phi < \pi$ is the active range where lock can be maintained. For the phase detector type shown (Gilbert multiplier or mixer), the voltage vs. phase slope reverses outside this

range. Thus the frequency would change in the opposite direction to that required to maintain the locked condition.

$$V_{e\text{-}max} = \pm K_D \, \pi/2$$

When the phase detector output voltage is applied through the loop filter to the VCO,

$$\Delta\omega_{out-max} = \pm K_V \, \pi/2 \; = \; \omega_L \;\; \text{(lock range)}$$

where $K_V = K_O \, K_D$, the product of the phase detector and VCO gains.

This is the frequency range around the free running frequency that the loop can track.
Doesn't depend on the loop filter
Does depend on DC loop gain

b. The lock range could also be limited by the tuning range of the VCO. Oscillator tuning range is limited by capacitance ratios or current ratios and is finite. In many cases, the VCO can set the maximum lock range.

6. Capture range: Range of input frequencies around the VCO center frequency onto which the loop will lock when starting from an unlocked condition. Sometimes a frequency detector is added to the phase detector to assist in initial acquisition of lock.

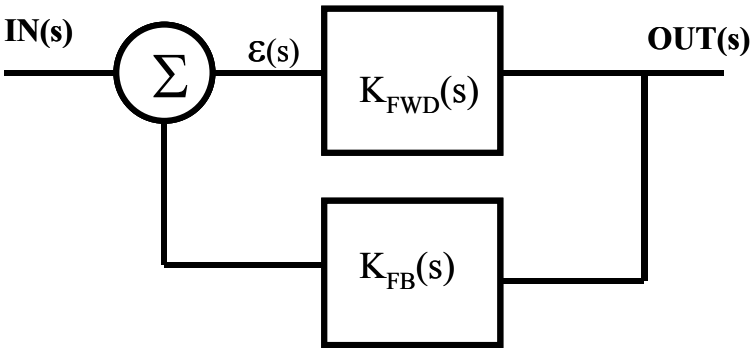
7. Approach: We will discuss the details of phase detectors and loop filters as we proceed. But, at this point, we will treat the PLL as a linear feedback system. We assume that it is already "locked" to the reference signal, and examine how the output varies with the loop transfer function and input. A frequency domain approach will be used, specifically describing transfer functions in the s-domain.

$$Ve(s)/\Delta\phi \; = \; K_D$$

$$\phi_{out}(s)/V_{cont}(s) \; = \; K_O/s$$

Note that the VCO performs an integration of the control voltage and thus provides a factor of 1/s in the loop transfer function. Because of this, a PLL is always at least a first order feedback system.

PLL is a feedback system



Loop Gain: $T(s) = K_{FWD}(s)\,K_{FB}(s)$

Transfer Function: $\dfrac{OUT(s)}{IN(s)} = H(s) = \dfrac{K_{FWD}(s)}{1 + T(s)}$

The Loop gain can be described as a polynomial:

$$T(s) = \frac{K'(s+a)(s+b)\cdots}{s^n\,(s+\alpha)(s+\beta)\cdots}$$

ORDER = the order of the polynomial in the denominator

TYPE = n (the exponent of the s factor in the denominator)

PHASE ERROR = $\varepsilon(s) = \dfrac{IN(s)}{1 + T(s)}$

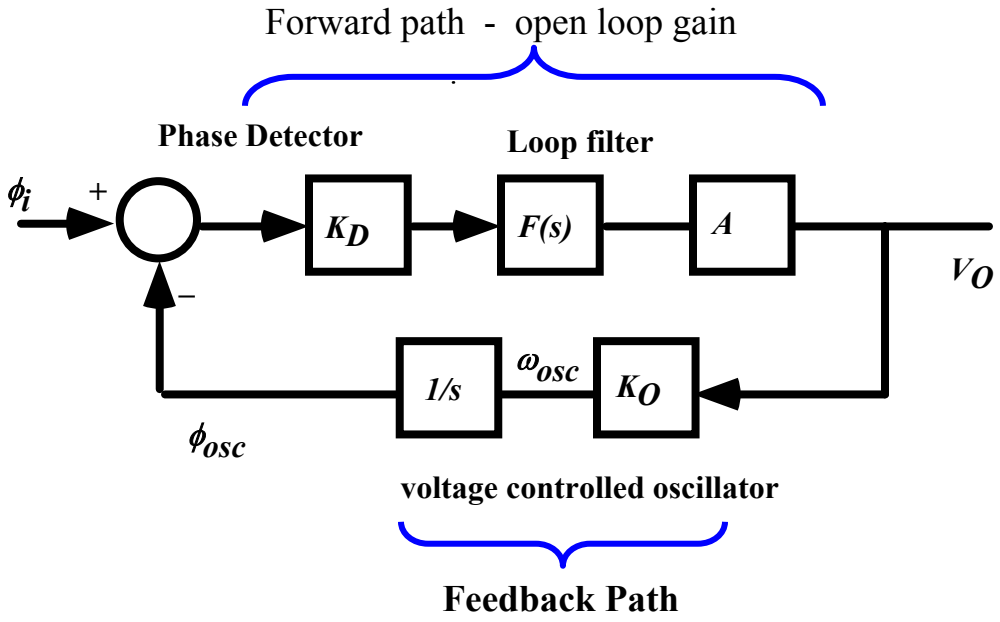
STEADY STATE ERROR = $\varepsilon_{SS} = \lim_{s \to 0}[s\varepsilon(s)] = \lim_{t \to \infty} \varepsilon(t)$

(this is the Laplace Transform final value theorem)

SS error is a characteristic of feedback control systems. This is the error remaining in the loop at the phase detector output after all transients have died out. Once again, you can see that a large loop gain T(s) leads to a small phase error.

A. FM Demodulator. (See Gray and Meyer, Chap. 10, Section 4.)

Our first application example is the FM Demodulator.



$$\frac{V_O}{\phi_i} = \frac{K_D F(s)\, A}{1 + K_D F(s)\, A(K_O / s)}$$

$$\frac{V_O}{\omega_i} = \frac{1}{s}\frac{V_O}{\phi_i} = \frac{K_D F(s)\, A}{s + K_D F(s)\, A\, K_O}$$

For convenience, we define $K_V = K_D K_O A$

How does the PLL work as an FM demodulator?

Frequency to voltage conversion: We need to convert the frequency variation of the input signal to a baseband signal whose frequency is equal to f_m, the modulation frequency, and whose amplitude is proportional to Δf, the frequency deviation. The input carrier frequency will be centered at the IF frequency, but will vary in time around this frequency.

Input Variable: $\omega_i = \omega_c + \Delta\omega \sin \omega_m t$

Output Variable: $V_O = \Delta\omega / K_O \sin \omega_m t$

In the FMD application, the output is the VCO control voltage, not the phase of the VCO. This voltage will track the input FM signal modulation frequency and deviation. The loop filter is lowpass. The block A represents a gain factor, usually 1 with a passive LPF, but it can be higher if the filter is implemented with an active filter.

Assume that the loop is locked at the IF frequency, ω_C. Frequency modulation will shift the instantaneous frequency around ω_C by $\Delta\omega$ at rate ω_m. As the frequency shifts with time, the phase detector will sense a phase error that increases with time. The filtered error voltage, $V_{cont} = V_O$, will send the VCO closer to $\omega_C + \Delta\omega$, tracking the frequency shift. If the bandwidth of the loop is greater than ω_m, the loop will track the frequency deviation of the input signal and V_O will be the demodulated baseband signal,

$$\Delta\omega/K_O \sin(\omega_m t).$$

Now we will consider the frequency and time response of a PLL in the FMD application. The loop filter transfer function F(s) has a big influence on these responses.

There are two typical applications.[1]

1. Analog baseband demodulation. This would be the case for an FM radio where speech or music is the baseband signal to be recovered.

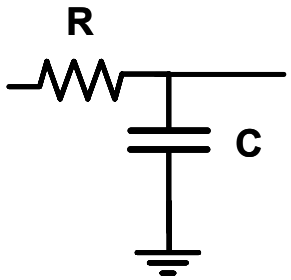
2. Digital demodulation. The simplest application of this is Binary FSK or Frequency Shift Keying. The frequency is changed in a binary step from f_{m1} to f_{m2} and back in order to transmit digital information.

[1] Note that there are many other techniques besides PLLs that are used to demodulate PM or FM signals, but this application of the PLL is a good one that helps to illustrate how they function.

We will start from the open loop gain, T(s).

$$T(s) = K_D F(s) K_O A/\text{s}$$

We know that the phase detector will be producing an output at twice the carrier or IF frequency, thus some low pass filtering will be needed. Let's start with a simple RC lowpass network.



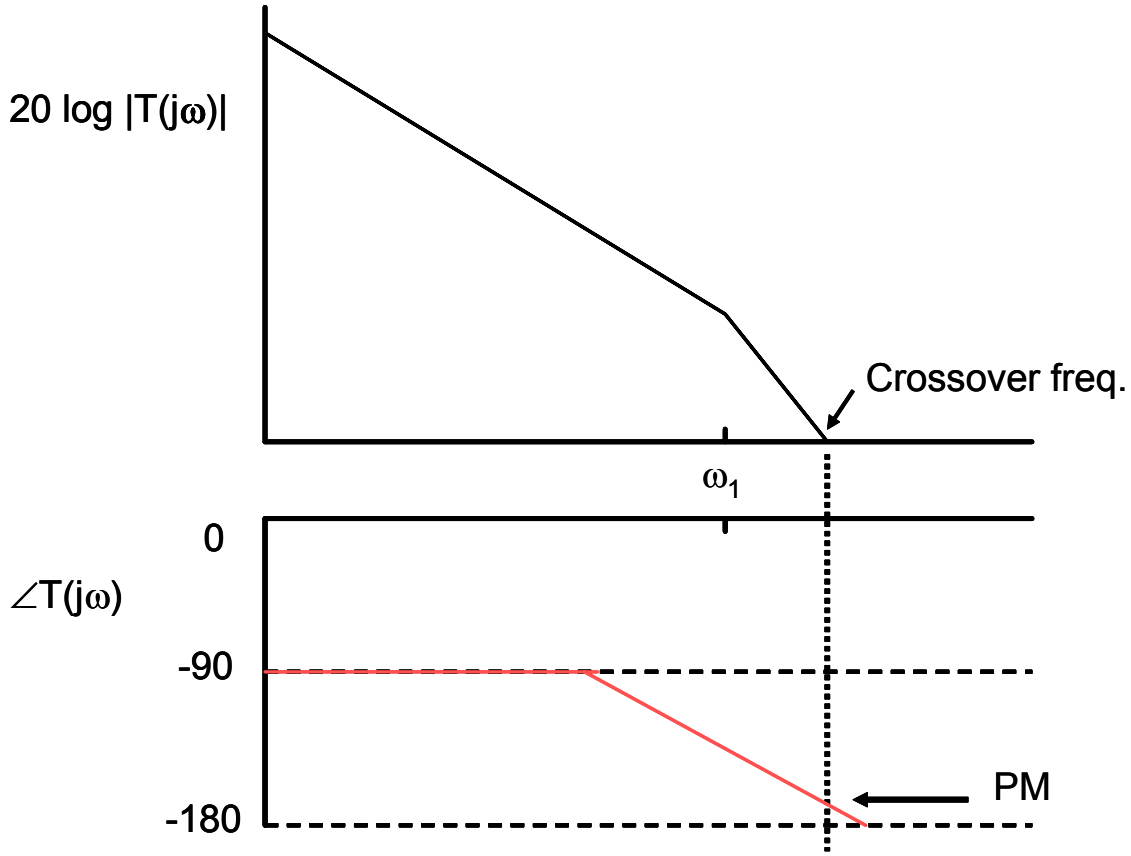
This network has a cutoff (3 dB) frequency $\omega_1 = 1/RC$. Thus, the filter transfer function is a simple lowpass,

$$F(s) = \frac{1}{1 + s/\omega_1} \ .$$

Then, T(s) becomes second order, Type 1:

$$T(s) = \frac{K_O}{s} \frac{K_D A}{1 + s/\omega_1} = \frac{K_V}{s(1 + s/\omega_1)}$$

Bode Plot: Now look at the Bode plot of T(jω).



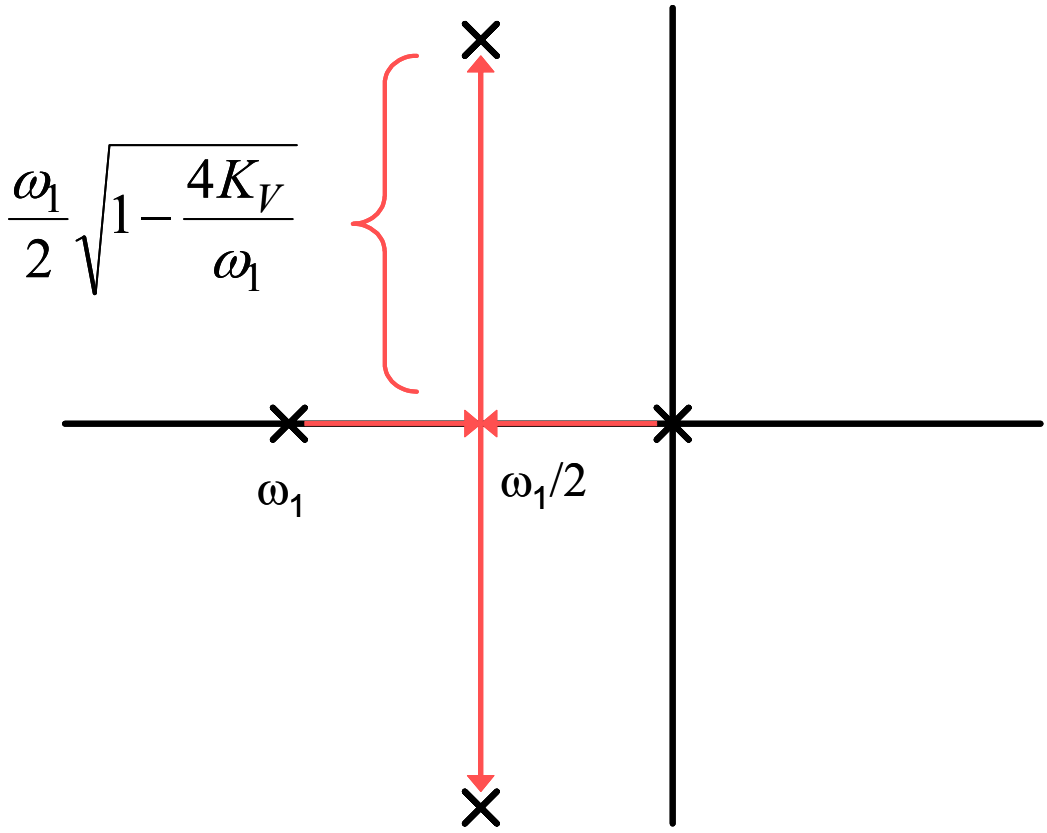
If the loop filter frequency is lower than the crossover frequency, then the phase margin can be unacceptably small. And, if we increase the loop gain, $K_V = K_D K_O A$, to reduce the residual phase error, we get even smaller phase margin. Thus, we have a conflict between stability of the loop and minimizing the phase error. However, the loop can be made to work if $\omega_1 > \omega_{crossover}$. But, then we may have insufficient filtering of the phase detector output.

Before we fix this problem, let's look at the root locus and then the closed loop response of this PLL.

Root Locus: The root locus represents the roots of the denominator of the closed loop transfer function. Set 1 + T(s) = 0 and solve for s as a function of K_V.

$$s = -\frac{\omega_1}{2}\left(1 \pm \sqrt{1 - \frac{4K_V}{\omega_1}}\right)$$

We see that as K_V is increased, the roots approach one another then become complex conjugates.



We can have a very underdamped response when $\omega_1 << K_V$. Think about the inverse Laplace transform of the complex conjugate pole pair.

$$e^{-\omega_1 t/2}\sin\left(\frac{\omega_1}{2}\sqrt{1-\frac{4K_V}{\omega_1}}\right)t$$

There is an exponentially decaying term determined by the real part of the roots that shows how long it takes the system to settle after a phase or frequency step and a ringing frequency dictated by the imaginary part of the pole pair. Again, when $\omega_1 << K_V$, we have a high ringing frequency and a long settling time, characteristic of a system that is not very useful.

Finally, it is sometimes useful to define a natural frequency, ω_n, and a damping factor, ζ. This is standard control system terminology for a second order system. The key is to put the denominator of the closed loop transfer function, 1 + T(s), into a "standard" form: either

$$s^2 + 2\zeta\omega_n s + \omega_n^2$$

or

$$\frac{s^2}{\omega_n^2} + \frac{2\zeta}{\omega_n} s + 1 \quad .$$

Taking the first formula, 1 + T(s) can be written as:

$$s^2 + \omega_1 s + K_V \omega_1$$

so, we can associate ω_n and ζ with:

$$\omega_n = \sqrt{K_V \omega_1}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_V}}$$

This form allows you to use standard equations and normalized plots to describe the frequency and transient response of the system. As we saw with the other ways of representing the frequency response of the system, a large K_V, which we like for reducing phase error, leads to a small ζ, which is bad for stability and settling time.

For example, the transient response for a Type 1, second order lowpass system such as this is plotted in the next figure taken from Motorola App. Note AN-535. It is clear that damping factors less than 0.5 produce severe overshoot and ringing.

In the frequency domain, the closed loop transfer function will also exhibit gain peaking when the system is underdamped. This is the same effect that we saw with feedback amplifiers.

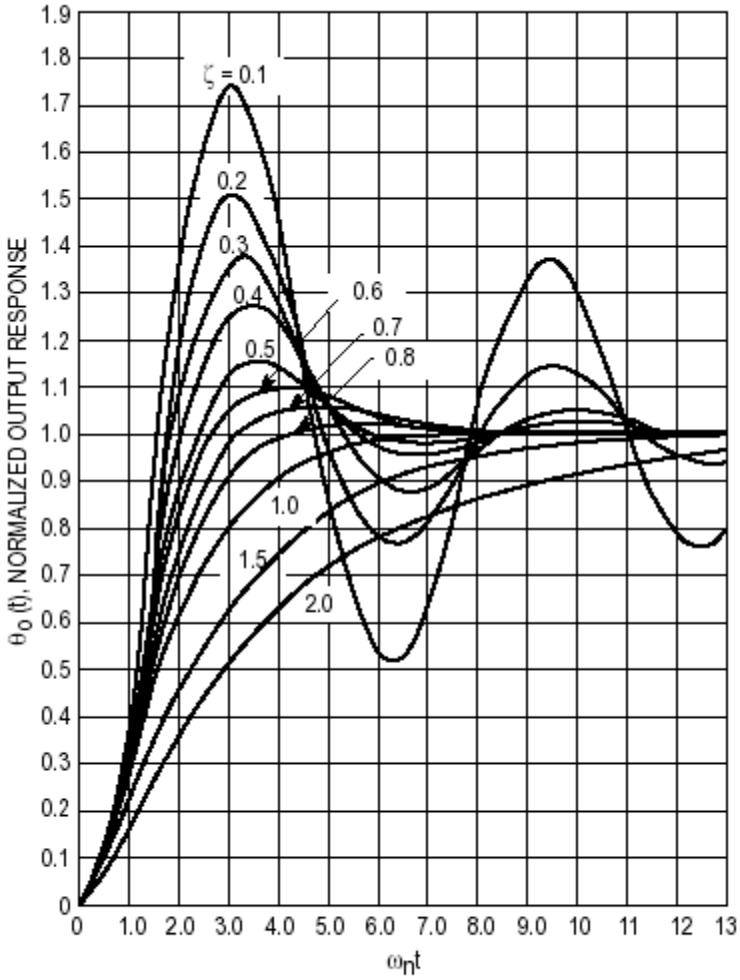
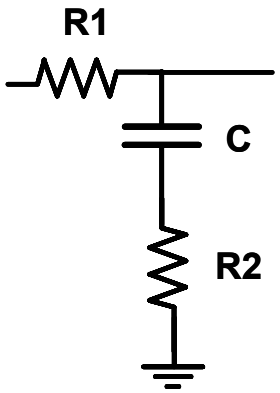


Figure 4. Type 1 Second Order Step Response

So, it is clear that we need a better transfer function that gives us more flexibility in determining the bandwidth of the filter and the stability of the system. You can't obtain a narrow loop bandwidth without reducing the phase margin/damping factor.

Add a zero to the loop filter transfer function to manipulate the root locus and improve stability.

Adding a resistor to the lowpass loop filter contributes a zero to its transfer function.



$$F(s) = \frac{1 + s/\omega_2}{1 + s/\omega_1}$$

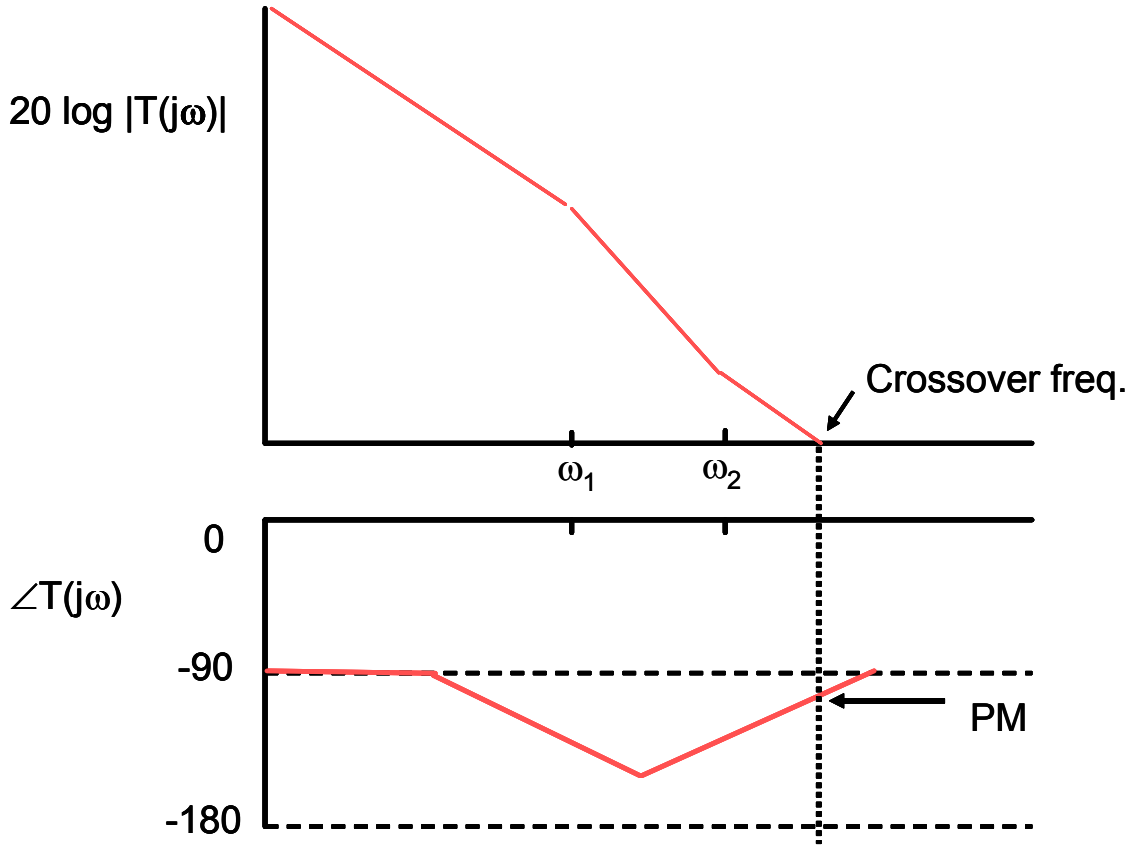
where

$$\omega_1 = \frac{1}{(R_1 + R_2)C}$$

$$\omega_2 = \frac{1}{R_2 C}$$

Thus, the zero frequency is always higher than the pole frequency.

Check out the Bode plot, root locus and transient response again.

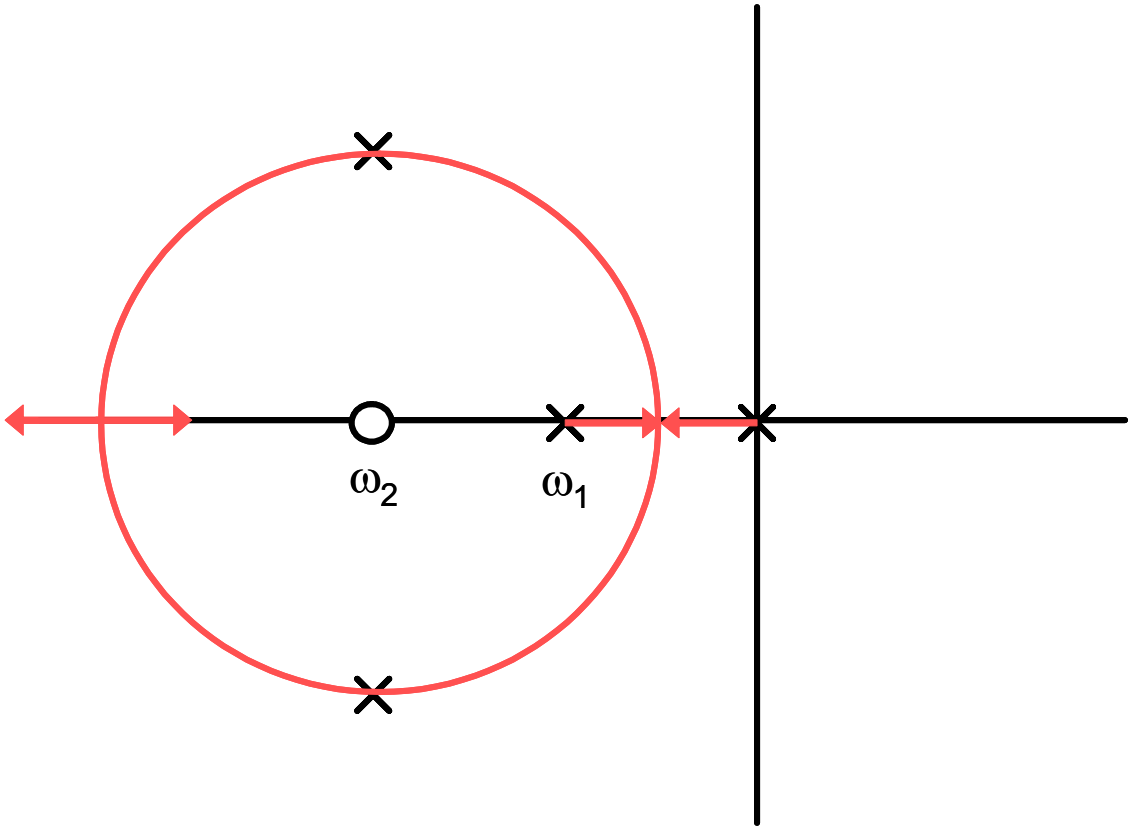


Note that the phase margin has increased. Now, small values of ω_1 can be used for narrower filter bandwidth, or higher K_V values can be used for lower phase error without sacrificing phase margin. Note how phase margin now improves when the crossover frequency is increased due to higher gain.

Root Locus: Calculate the closed loop transfer function for this PLL with the pole-zero loop filter.

$$\frac{V_O(s)}{\omega_{in}} = \frac{1}{K_O} \frac{1 + s/\omega_2}{\frac{s^2}{K_V \omega_1} + \left(\frac{1}{K_V} + \frac{1}{\omega_2}\right)s + 1}$$

The denominator is of the form 1 + T(s). Solve for the roots; these are the poles. The zero changes the root locus into a circle as K_V becomes large. Note that this has the advantage that the poles move away from the jω axis thereby improving damping, reducing settling time and stability. Eventually the roots rejoin the real axis, and the transient response becomes overdamped.



We can also extract ω_n and ζ from the closed loop transfer function since the denominator is in one of the standard forms.

$$\omega_n = \sqrt{K_V \omega_1}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_V}} + \frac{1}{2}\frac{\omega_n}{\omega_2}$$

We see that ω_n is the same as with the simple RC filter, but the damping factor has an added term. The first term is quite small in most cases, but the second term can be made large by increasing K_V or reducing ω_2. We still have a type 1 system, but we have an added term that we can use to improve stability, the zero frequency. Note that the zero will also affect the frequency and transient response as was shown in our discussion of feedback amplifiers. It generally helps, but now we can't use all of the formulas in Lee's handy table.

FREQUENCY RESPONSE

According to Gardner[2], the loop bandwidth for this Type 1, second-order loop with a forward path zero is given by:

$$\omega_h = \omega_n \left[1 + 2\zeta^2 + \sqrt{(1 + 2\zeta^2) + 1} \right]^{1/2}$$

According to this, we have a bandwidth of about $2\omega_n$ for $\zeta = 0.707$.

Refer to Fig. 2.3 from Gardner. This is a plot of the closed loop frequency response of a high gain second order PLL: $20 \log |H(j\omega)|$. A high gain PLL is defined by $K_V/\omega_2 >> 1$.

F.M. Gardner, Phaselock Techniques, Wiley 1979.

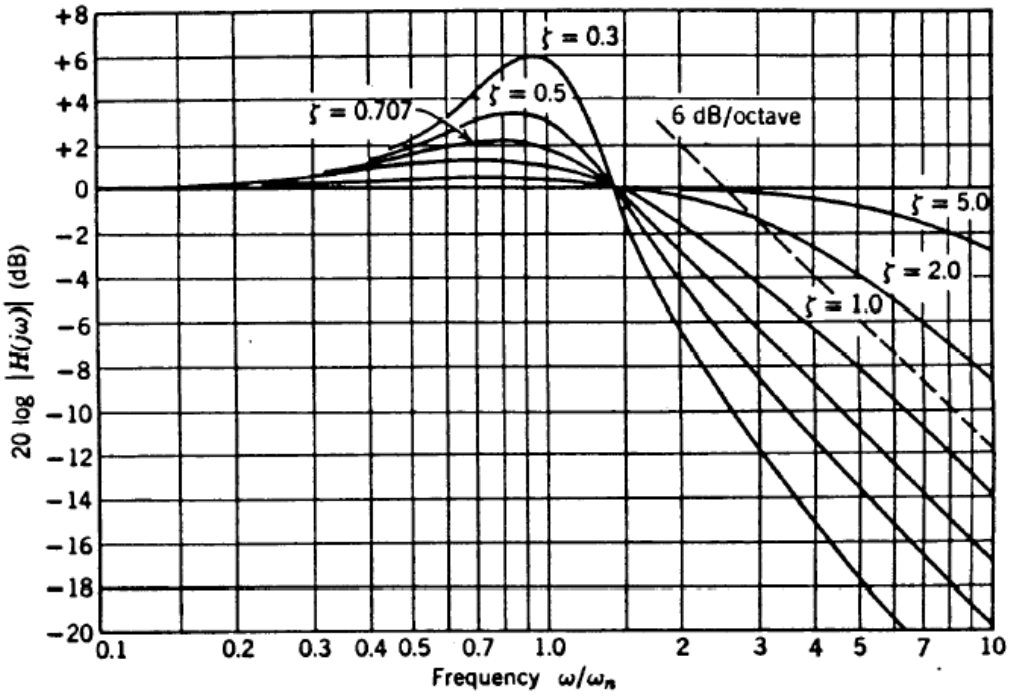


Figure 2.3 Frequency response of a high-gain second-order loop.

[2] F. M. Gardner, Phaselock Techniques, Second ed., Wiley, 1979.

From this plot, we can see how the 3 dB frequency and gain flatness varies with ζ. Also, we see that the natural frequency must be significantly greater than the maximum frequency component (maximum modulation or baseband frequency for the FM demodulator application; frequency of phase variation for the synthesizer) at the input when $\zeta < 1$ in order to avoid gain peaking. This is a consequence of the zero added to the transfer function. For applications that require very small gain peaking (such as clock recovery), $\zeta > 2$ is often employed.

PHASE ERROR

There is no frequency error when the loop is locked

- Input frequency = output frequency

But, it is possible to have a phase error for some input transient phase conditions. The phase error must remain bounded in order to keep the loop locked. To analyze in the frequency domain, we assume a sinusoidal phase variation at the input.

PHASE ERROR = $\varepsilon(s) = \dfrac{IN(s)}{1 + T(s)}$

STEADY STATE ERROR = $\varepsilon_{SS} = \lim_{s \to 0}[s\varepsilon(s)] = \lim_{t \to \infty} \varepsilon(t)$

Fig. 2.4 from Gardner's book illustrates how the phase error, expressed as

$$\varepsilon(s) = 20 \log (\phi out/\phi in) \quad dB$$

increases as the input frequency approaches the natural loop frequency for the case with $\zeta = 0.707$. For input phase variations well below the loop bandwidth, the loop tracks very well. This is because |T(jw)| is large at low frequency.

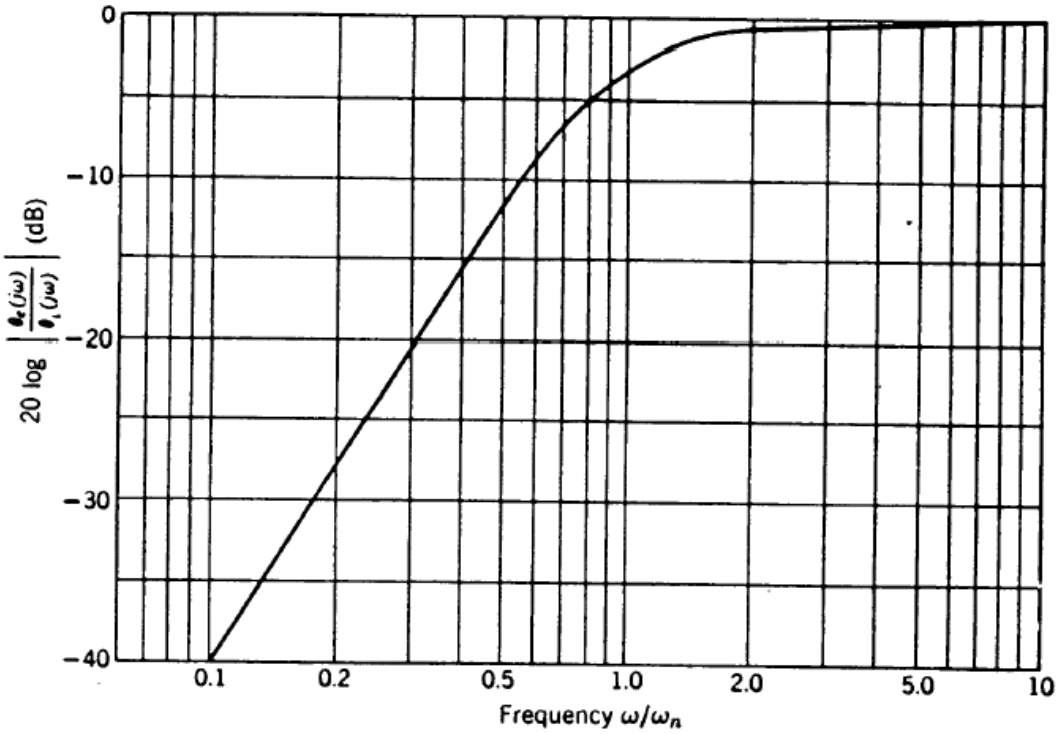


Figure 2.4 Error response of high-gain loop, $\zeta = 0.707$.

TRANSIENT PHASE ERROR

- Inverse Laplace transform of ε(s)

Now, let's look more closely at how the phase error is affected by the type of transient phase signal at the input of the Type I PLL.

1. Phase step. Because $\phi_{in}(t) = \Delta\theta\, u(t)$, in the frequency domain,

$$\phi_{in}(s) = \frac{\Delta\theta}{s}$$

The steady-state phase error can be calculated from ε(s) and εss above.

$$\varepsilon_{ss} = \lim_{s \to 0} \frac{s\dfrac{\Delta\theta}{s}}{1 + \dfrac{K_V}{s}\left(\dfrac{1 + s/\omega_2}{1 + s/\omega_1}\right)} = 0$$

Thus, there is only a transient phase error for a phase step. This is reasonable, because the control voltage must return to the same value after the phase step is completed. The frequency will be the same before and after the step.

2. Frequency step.

$$\varepsilon_{ss} = \lim_{s\to 0} \frac{s\dfrac{\Delta\omega}{s^2}}{1+\dfrac{K_V}{s}\left(\dfrac{1+s/\omega_2}{1+s/\omega_1}\right)} = \lim_{s\to 0} \frac{\Delta\omega}{s+K_V\left(\dfrac{1+s/\omega_2}{1+s/\omega_1}\right)} = \frac{\Delta\omega}{K_V}$$

There is a static "error", but it can be made small by increasing K_V. This is consistent with the idea that a shift in control voltage is needed to give a step in frequency. The phase error needed to generate this control voltage step varies inversely with the loop gain.

3. Frequency ramp. We could do the same exercise for a frequency ramp (Doppler shift). This gives an unlimited steady state error. So, a type I loop is not suitable for tracking a moving source.

Summarizing:

Type I; second order: $F(s)=\dfrac{1+s/\omega_2}{1+s/\omega_1}$

Input	$\phi_{in}(s)$	ε_{ss}
Phase step	$\Delta\theta/s$	0
Freq. step	$\Delta\omega/s^2$	$\Delta\omega/K_V$
Freq. ramp	A/s^3	infinite

In the demodulator application, we can see that the Type 1 second-order PLL will give zero steady state phase error for a PSK input (thus, it isn't useful as a PSK demodulator) and finite phase error for an FSK input if frequency deviation $\Delta\omega$ is small and K_V is large, but will have unbounded error for a constantly drifting frequency such as might be caused by the Doppler effect on a moving signal source.

Sinusoidal baseband modulation

Figure 4.1 from Gardner plots the steady state phase error for a frequency modulated source with a single frequency sinusoidal baseband signal. Note that this error is normalized to the ratio of the frequency deviation $\Delta\omega$ to the loop natural frequency.

Looking at this from a slightly different perspective, suppose that we have a sinusoidal FM source with modulation frequency ω_m and deviation $\Delta\omega$. We see that the steady state phase error can be small if ω_m/ω_n is small and $\zeta > 0.7$.

The steady state phase error can be read from the plot:

$\varepsilon_{ss} = \theta_e = (\Delta\omega/\omega_n)$ x (normalized phase error from the plot)

This steady state phase error must remain within the operational range of the phase detector or the loop will lose lock.

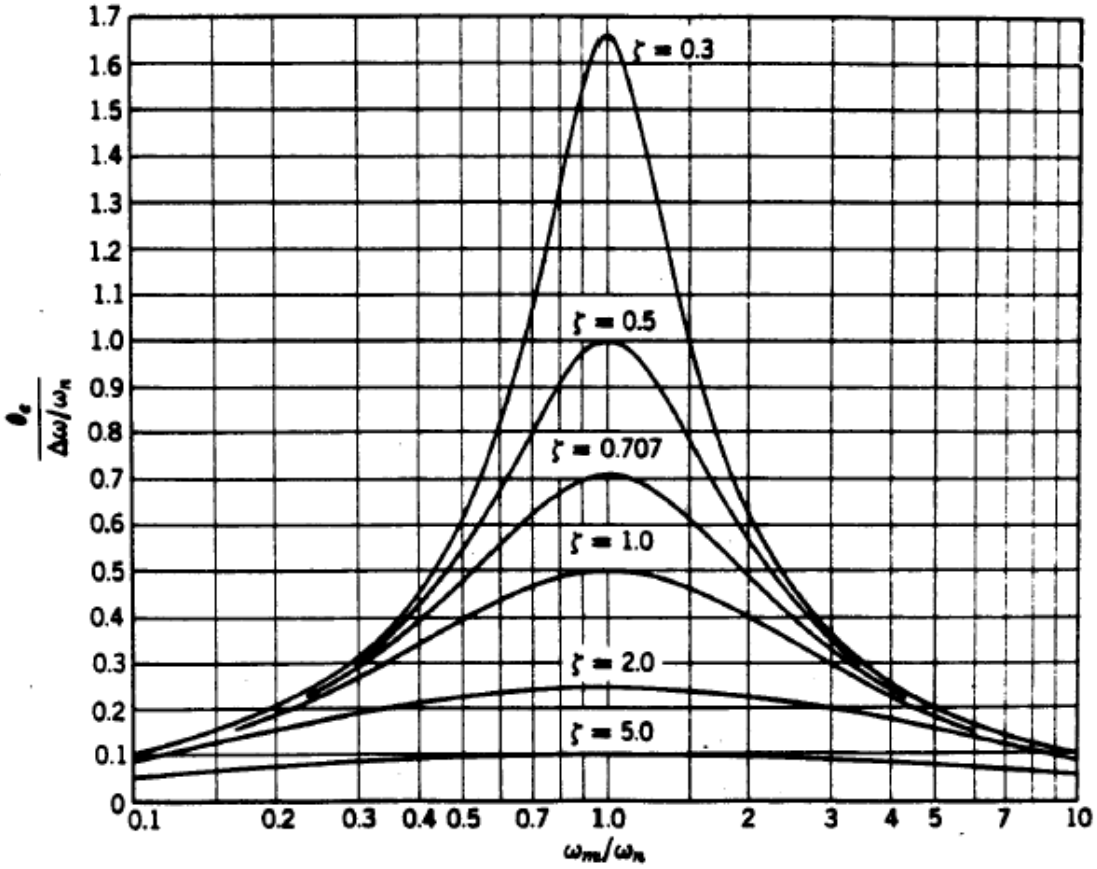


Figure 4-1 Steady-state peak phase error due to sinusoidal FM. (High-gain, second-order loop.)
By permission of L. A. Hoffman.

Example. **FM broadcast application.**

Channel bandwidth	200 kHz
Maximum modulation frequency	$\omega m,max = 2\pi$ x 15 kHz = 9.4 x 10^4 rad/s
Maximum frequency deviation	$\Delta\omega$, max = 2π x 75 kHz = 4.7 x 10^5 rad/s

1. Determine K_V. Let's use rough numbers just for illustration
   phase detector gain = 1 volt/rad
   VCO gain = 10^7 rad/s/volt

So, $K_V = 10^7\ s^{-1}$

2. To obtain low phase error and small gain peaking, we need $\omega_n >> \omega_{m,max}$

   arbitrarily choose $\omega_n = 5\ \omega_{m,max}$

then the pole frequency, $\omega_1 = \omega_n^2/K_V = 2.2 \times 10^4$ rad/s is determined.

From Fig. 4-1, this gives us a maximum transient phase error of

$$\theta_e = 0.2\ \frac{\Delta\omega}{\omega_n} = 0.2 \text{ radians.}$$

3. choose ζ. Then, ω_2 can be calculated:

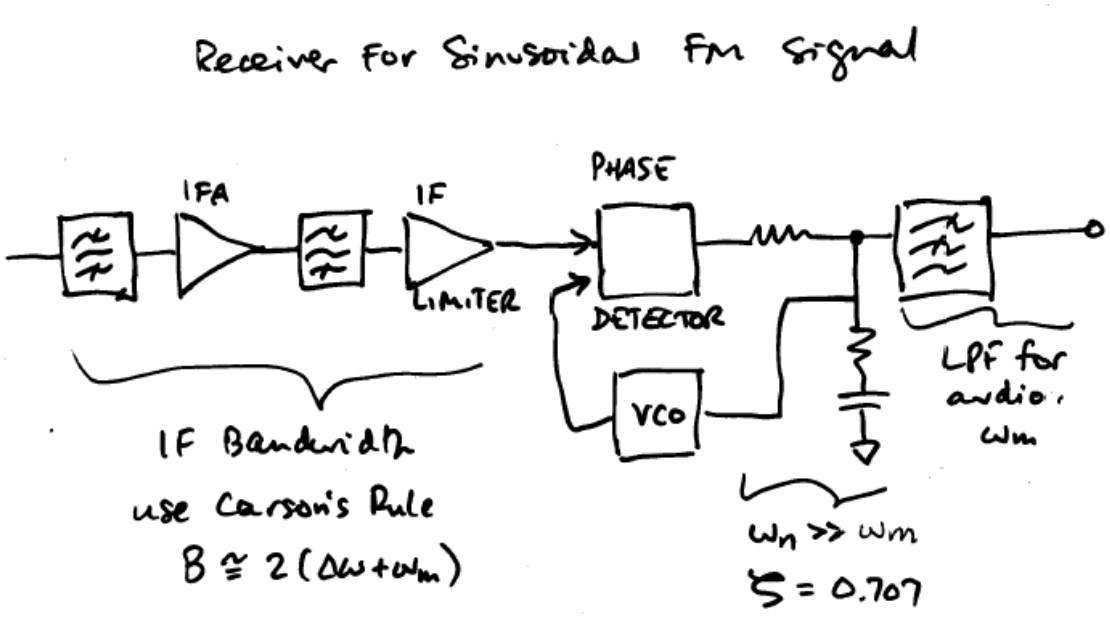
$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_V}} + \frac{\omega_n}{2\omega_2}$$

Typically the second term is much larger than the first.

Let $\zeta = 0.707$. Then $\omega_2 = \omega n/2\zeta = 3.4 \times 10^5$ rad/s

4. Check the maximum steady state phase error for this case. From the plot, we have a normalized value = 0.2 for $\omega_n/\omega_m = 0.2$. Thus, $\varepsilon_{ss} = 0.2$ radians since $\Delta\omega/\omega_n = 1$ in this example. This should be well within the operating range of most phase detectors.

Here is a block diagram of the IF and demodulator sections of an FM receiver.



Frequency shift keying: In FSK we have a frequency step. We know that the steady state phase error is bounded when KV is large, but we should also consider the peak transient phase error. If this exceeds the phase detector operating range, we may lose lock and skip cycles before lock is recovered. Referring to Gardner again, Fig. 4.3 shows the transient phase error for a frequency step.

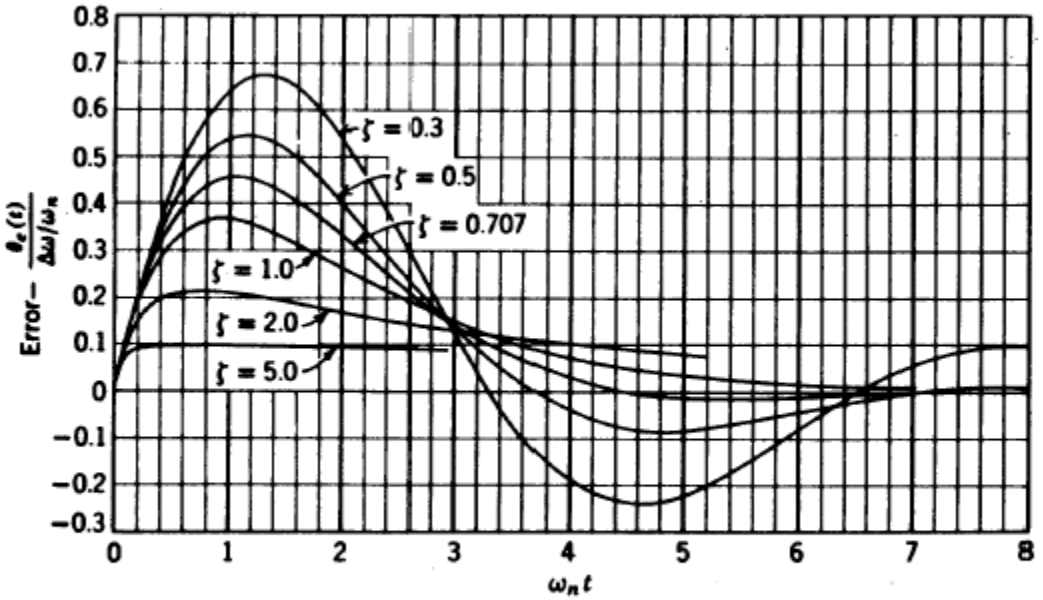


Figure 4-3 Transient phase error $\theta_e(t)$ due to a step in frequency $\Delta\omega$. (Steady-state velocity error, $\Delta\omega/K_v$, neglected.) By permission of L. A. Hoffman.

The worst case overshoot is close to $\omega_n t = 1$. With $\zeta = 0.707$, $\theta_e/(\Delta\omega/\omega_n) = 0.45$.

If $\Delta\omega$ = frequency step size (deviation) and $\theta e,max = \pi/2$ radians, we can determine a minimum value of ω_n to avoid losing lock.

$$\omega_n \geq 0.45 \frac{\Delta\omega}{\theta_e} = 0.29\Delta\omega$$