How To Design RF Circuits - Synthesisers

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Introduction

Frequency synthesisers form the basis of most radio system designs and their performance is often key to the overall operation. This paper will present an introductory overview of the basic parameters governing the design of a phase locked loop frequency synthesiser and their effects, with the sources of phase noise within a design also being considered. Finally a list of common problems, along with some possible solutions, is given in order to assist in the de-bugging of a non-functional design once assembled.

What is a Synthesiser?

A synthesiser is a device which takes an input, or source, frequency and from it produces an output frequency which is either directly or indirectly related to it. Possible schemes for direct and indirect synthesisers are shown in figure 1.

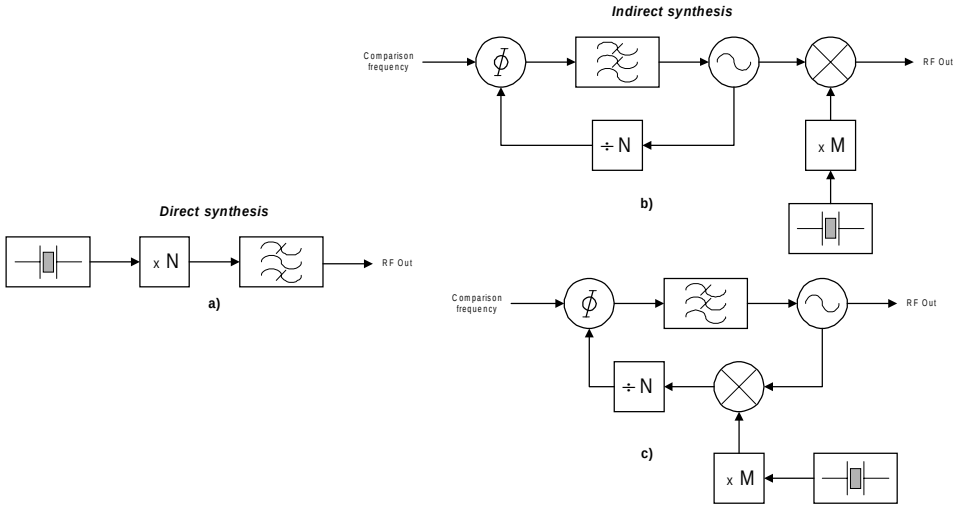

Figure 1 : Direct and indirect synthesisers.

The direct synthesiser, figure 1a), produces an output which is directly proportional to the input, i.e. for an input frequency f_{IN} and a multiplication factor of N, then the output frequency f_{OUT} is given as

$$f_{OUT} = N \cdot f_{IN} \qquad \textit{Equ. 1}$$

where N can be a fractional value (e.g. ¼) as well as an integer value. Combinations of fractional and integer multipliers between the synthesiser frequency source and the output can produce output frequencies with strange multiples such as 10¾. It should be noted that the "multiplier" can be formed of one or more elements. Figure 2 shows how a "x3" multiplication may be done.

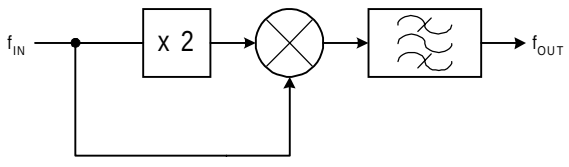

Figure 2 : "x3" multiplier.

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In both the direct and indirect synthesisers shown, it may be necessary to have some form of output filtering. This would ensure that harmonics and other related spurious frequencies, which may cause spurious responses in a receiver or compression in a transmitter power amplifier, are kept to a sufficiently low level.

Indirect synthesisers, shown in figure 1b) and c), operate by "locking" the output of a frequency source, usually a VCO, to that of another, "cleaner" source, know as the reference frequency. The reference frequency usually has better phase noise, particularly at low frequency offsets, and is more stable in terms of drift with temperature, vibration, etc. The additional mixing stages allow for the generation of frequencies which are higher, but require a fine step tuning range. The benefits of this will be addressed later.

Figure 3 shows the basic block diagram of a phase locked loop. The VCO is "locked" to the reference frequency, f_{ref}, by dividing the reference, f_{ref}, by some integer R, the VCO output, f_{out}, by some integer N, and then comparing the phase of the two signals, generating an error signal. This error signal is then amplified and filtered to remove phase comparison frequency components and modify the phase response of the loop to provide closed loop stability. It is almost always the case that the reference is a higher quality frequency source than the VCO. The output frequency is then given by

$$f_{out} = \frac{N}{R} \cdot f_{ref} \qquad \textit{Equ. 2}$$

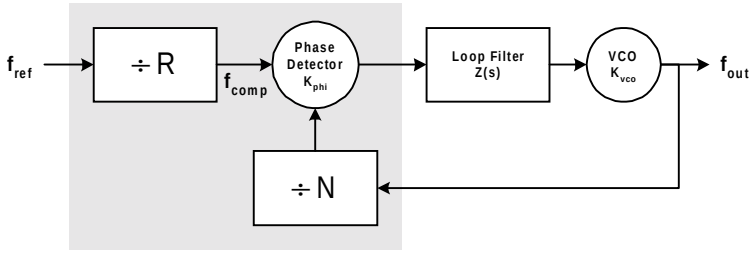

Figure 3 : Basic diagram of a phase locked loop.

The shaded area of figure 3 is usually integrated into a synthesiser IC, although in special cases some or all of these components can be designed as application specific elements, e.g. the N and/or R divider created from ECL logic D-types.

Phase Detector Types

The phase detector in a PLL can take many forms, such as an XOR gate (Type 1), a mixer (Type 1) and Dual D-Types (Type 2) amongst many, although the latter is probably the most common. The type is usually predetermined if a single chip synthesiser is used, however for some applications they can be designed using suitably fast logic, such as that used for a divider, although the operational speed requirement is not as severe.

For the purposes of this paper, as it deals mainly with integrated synthesisers, references to the phase detector will be assumed to also refer to the action of the charge-pump output used to tune the VCO via the loop filter. However, it should be noted that not all phase detectors have a current output; some have voltage outputs which will change the procedure for the design of some of the loop components, such as the passive loop filter.

Division In The Loop

Fixed division dividers

In a loop where the frequency input exceeds either the maximum RF or reference input frequency of a synthesiser it may be necessary to use a fixed divide by M prior to the ÷N or ÷R functions. M has been used to highlight the difference between M and N. N will be referred to as the division performed by the synthesiser IC used to form the basis of the PLL. The value of M will however limit the step size the synthesiser may perform as the output frequency will now be, assuming the M division is prior to the ÷N, of the form

$$f_{out} = \frac{M \cdot N}{R} \cdot f_{ref} \qquad \textit{Equ. 3}$$

This results in a minimum step size of $M*f_{comp}$. For a fixed division of M=8 and an N range of 3 to 65535, only division ratios of 24, 32, 40,…,524280 can be achieved. If this formed part of synthesiser trying to step in 8kHz, then the phase detector comparison frequency would have to be ≤1kHz.

Dual modulus prescalers

Dual modulus prescalers are a simple way of implementing a high frequency ÷N within a PLL. The division ratios commonly available are 8/9, 16/17, 32/33, 64/65, although using sufficiently fast logic, such as ECL, it is possible to build prescalers of other ratios. Figure 4 shows a general implementation of a dual modulus prescaler.

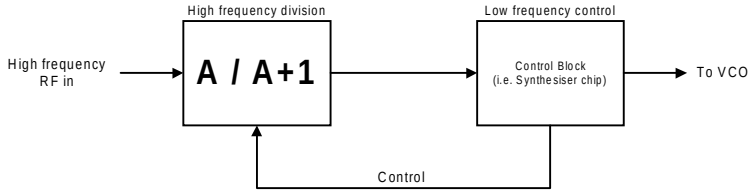

Figure 4 : Application of a dual modulus prescaler.

The use of a dual modulus prescaler presents a particular limit on the division possible within a loop. For a prescaler with division ratios of A and A+1 the minimum division ratio above which all N values can be accommodated is (A·(A-1)), i.e. for an 32/33 prescaler the minimum division from which continuous division is available is (32·(32-1)) = 992. Some divisions below 992 are possible, but need to be confirmed. This is an important point, as many synthesiser ICs now incorporate a dual modulus prescaler (e.g. LMX233x series from National Semiconductor and the ADF41/42xx series from Analog Devices).

Mixers in the division feedback loop

Mixers can be used to aid the division in the feedback loop as shown in figure 1c). The mixer essentially provides a down-conversion in the loop which lessens the amount of actual division required to synthesise the required output. For a reference frequency f_{ref}, the division ratios of N and R, and the frequency f_{mix}, applied to the mixer to down-convert the signal; the resulting output frequency, f_{out}, will be

$$f_{out} = \left(\frac{N}{R} \cdot f_{ref} \right) + f_{mix} \qquad \textit{Equ. 4}$$

The main benefit of this method is the improved noise performance due to the reduced division in the loop.

Loop Filter Design

3rd Order Passive Loop Filter

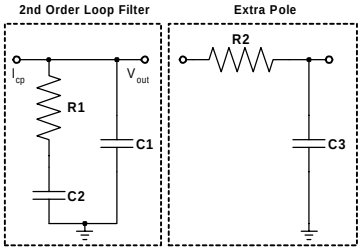

Figure 5 : A third order loop filter.

Figure 5 shows the standard third order loop filter used in most synthesisers. This comprises a second order filter section and an RC section providing an extra pole to assist the attenuation of the sidebands at multiples of the comparison frequency that may appear. The values for these components are easily calculated using the following equations [1]

$$C2 = \frac{K_{vco} \cdot I_{cp}}{\omega_{BW}^2 \cdot N} \qquad \textit{Equ. 5}$$

$$R1 = 2 \cdot \rho \cdot \sqrt{\frac{N}{K_{vco} \cdot I_{cp} \cdot C2}} \qquad \textit{Equ. 6}$$

$$C1 = \frac{C2}{12} \qquad \textit{Equ. 7}$$

$$C3 = \frac{R1 \cdot C2}{20 \cdot R2} \qquad \textit{Equ. 8}$$

$$R2 = 3 \cdot R1 \qquad \textit{Equ. 9}$$

where ρ is the damping factor and $\omega_{BW} = 2*\pi*f_{BW}$.

Other sources of equations for designing loop filters are also available such as [2], with comprehensive derivations of many other forms of loop filter given in [3].

Active Filters

If the tuning voltage required for the VCO is higher than the output range of the synthesiser charge-pump, another option is to use an active filter which runs off a higher power supply voltage. An active, third order loop filter is shown in figure 6.

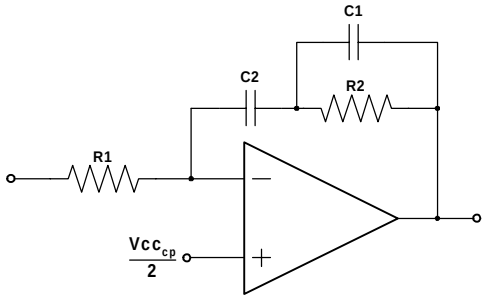

Figure 6 : Active third order loop filter.

$$F(s) = \frac{-1}{sC_1R_1} \cdot \frac{sR_2(C_1 + C_2) + 1}{sC_2R_2 + 1} \qquad \textit{Equ. 10}$$

The transfer function of the filter in figure 6 is given by equation 10 [3]. It is also possible to use an op-amp purely as a voltage amplifier following a loop filter of the type shown in figure 5. Great care should be taken when using op-amps as loop filters or amplifiers, as they can add significant noise to the synthesiser.

Design Example

The following is a basic specification for a frequency synthesiser

Specification	**Requirement**
Frequency tuning range	2.33GHz ± 50MHz
Step size	500kHz
Phase error contribution	≤ 3° rms
Lock time	≤ 400µs for a ±20MHz step to ≤ ± 200Hz of final frequency.

From these few parameters, we first need to estimate the loop bandwidth of the synthesiser. Two "rules of thumb" [4], which may help to approximate the frequency of the loop bandwidth, are

$$Switching\ \ time \approx \frac{50}{f_{comparison}} \qquad \textit{Equ. 11}$$

$$Switching\ \ time \approx \frac{2.5}{f_{loop\ bandwidth}} \qquad \textit{Equ. 12}$$

From equation 11, the estimated comparison frequency is ≥125kHz. As this is below the synthesiser step size, the comparison frequency will be set to 500kHz which easily meets the requirements of equation 11. With the required switching speed being <400µs, equation 12 predicts an estimated loop bandwidth of ≥6.25kHz in order to achieve lock in time. To ensure the requirement of equation 12 is met with margin, the loop bandwidth will be set to 10kHz.

Where switching time is unimportant, choice of loop parameters will be governed by phase noise and spurious requirements alone.

The follow sections will deal with each of the topics using this specification for all modelling and designs. Using equations 5 to 9, with some of the following details of the synthesiser, VCO and loop parameters

Synthesiser	Analog Devices ADF4212 [5]
Charge pump current (I_{cp})	5mA
K_{vco}	45MHz/V
Division range (N)	4560 to 4760
Reference frequency (f_{ref})	10MHz
Phase margin	45° ($\therefore \rho = \sqrt{2}$)

the component values for the complete loop filter shown in figure 5 are calculated to be

C1 = 1nF C2 = 12nF C3 = 180pF
R1 = 1.8kΩ R2 = 5.6kΩ

Open Loop Analysis

In order to have confidence in the stability of the synthesiser, an open loop analysis is performed to estimate the gain and phase margins. The analysis of theses parameters was performed using the ICAP/4 Windows spice simulator by Intusoft. Similar simulations have been carried out, with the same degree of success using Mathcad, Matlab and MS Excel.

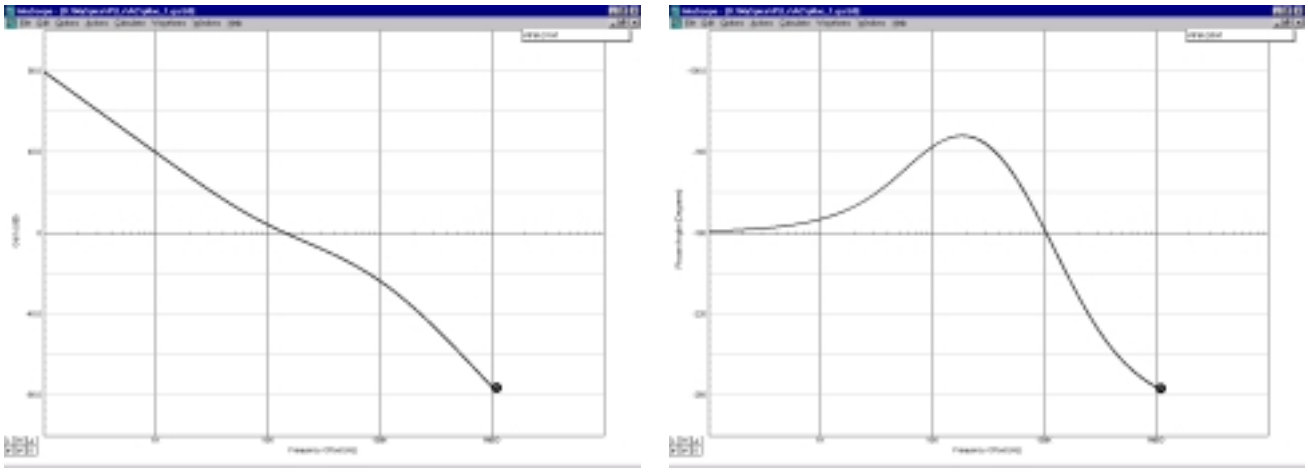

Figure 7 : Bode plots showing open loop gain and phase.

The gain margin is defined as the **magnitude** of the reciprocal of the open-loop transfer function at the frequency where the phase angle is -180°, and is a relative measure of stability. From the phase plot in figure 7 we see there is 180°

phase shift at ≈100kHz. The gain margin is the value at this offset on the gain plot of figure 7. In general it is desirable for this value to be greater than 15dB, the reading in this case being ≈25dB.

The phase margin is defined as **180° plus** the phase angle of the open loop transfer function at 0dB, or unity, gain. This is also a measure of relative stability. From the gain plot in figure 7, we can see that 0dB gain occurs at ≈13kHz, which corresponds to a phase margin of ≈48°. Phase margin values of ≥30° are usually sufficient.

Closed Loop Analysis

Frequency Response

To check that the closed loop performance is approximately that required we can analyse the frequency response of the loop. This was also performed using spice, the circuit diagram of which is shown in figure 8. This is a very simple model of a PLL, in fact the open loop analysis was done with the same circuit, with the link back to the phase detector model broken in order to "open" the loop. However, this linear approximation provides an adequate model of a PLL in order to have confidence that the design is close to that required. As with the open loop response, the simulation of the closed loop can be done using Mathcad, Matlab or MS Excel.

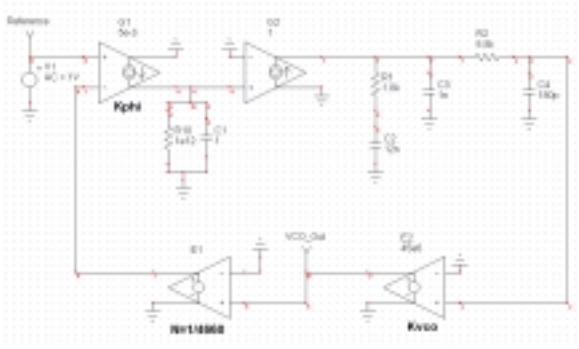

Figure 8 : Closed loop spice simulation of PLL synthesiser.

Figure 9 shows the closed loop frequency response of the synthesiser. This shows the gain response peaking, at about 3.3dB, at the loop bandwidth of 10kHz. If the peak is at 3dB, then this is an indication that the phase margin is 45°. Much greater peaking can be an indication of too little phase margin.

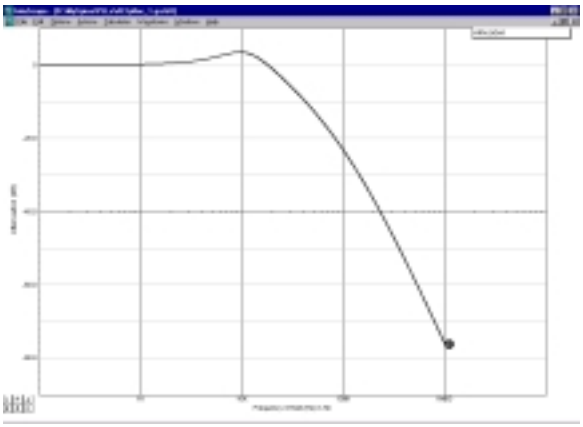

Figure 9 : Closed loop frequency response of figure 8.

For a detailed analysis of both open and closed loop responses refer to [6].

Transient Response

Figure 10 shows the transient response of the synthesiser to a step change in frequency of 20MHz. The y-axis is scaled in 1kHz/division, centred on 20MHz. The y-axis of the plot has been normalised to the final frequency of the VCO after the step response has been applied. The step response is applied at t=100µs. From this it is apparent that the loop has settled to the requirement of ≤200Hz of final frequency at ≈320µs.

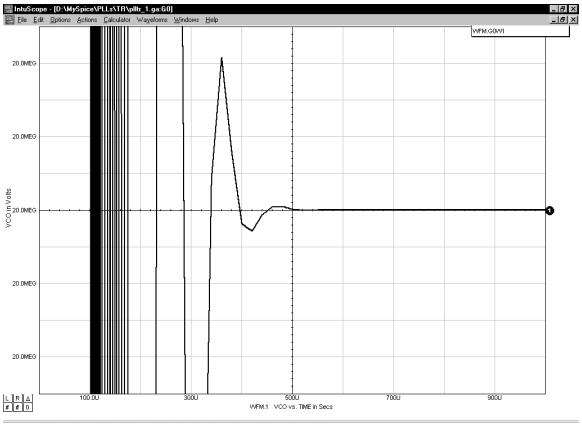

Figure 10 : Synthesiser transient response.

Measurements of the actual synthesiser indicate that, for a frequency excursion of ±20MHz, the lock time is ≈150µs, which is well below both the simulated value and the requirement.

A plot of the synthesiser output at 2.33GHz is shown in figure 11. The effect of the PLL is clearly visible as "shoulders" starting at the loop bandwidth, 10kHz.

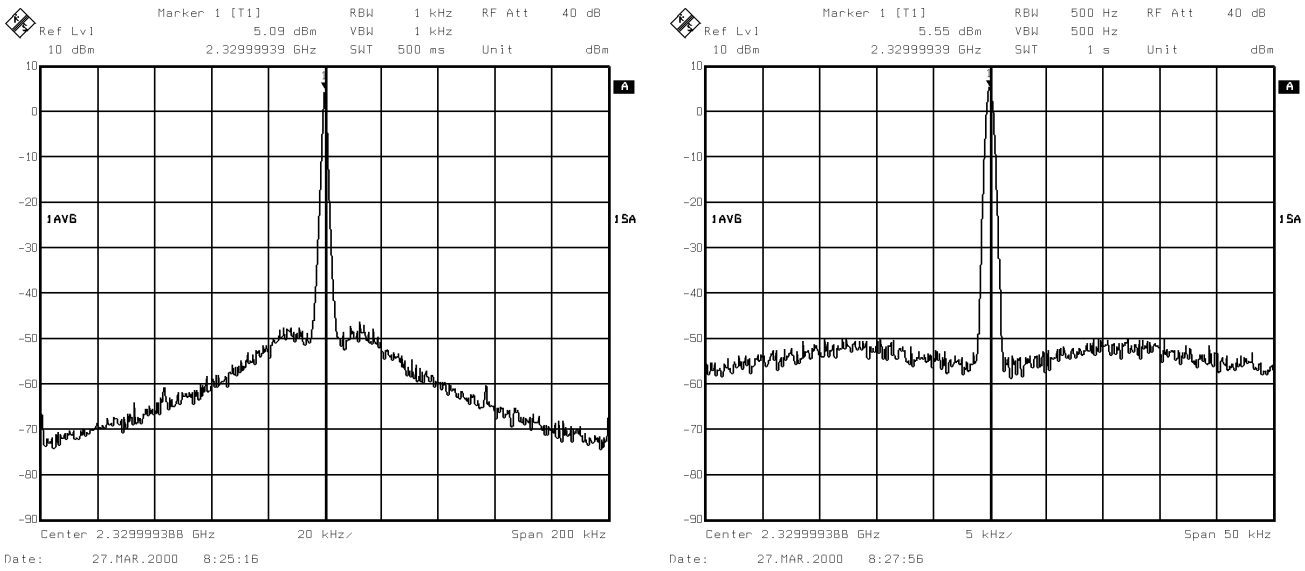

Figure 11 : Synthesised 2.33GHz spectrum.

Phase Noise

What is phase noise?

Although a full treatment is beyond the scope of this paper, the simple definition of phase noise used in this paper is that it is the energy introduced to the spectrum of an oscillator at frequency offsets either side of a carrier frequency, f_c, due to the effects of random phase and frequency modulation. Thinking of a perfect sine wave, imagine that the zero crossing points are not consistent and instead have a random element to their position. This randomness will spread the spectrum of the sine wave, such that the spectrum no longer looks like a single line, see figure 12. The four major causes [3] of phase noise in oscillators are f^{-1} noise or flicker noise, thermal FM noise, flicker phase noise and the thermal noise floor, although there are other contributions.

Referring to figure 12, we can see the "perfect" frequency source f_c (i.e. a single line), the typical phase noise profile of an oscillator and the single sideband noise power in a 1Hz bandwidth.

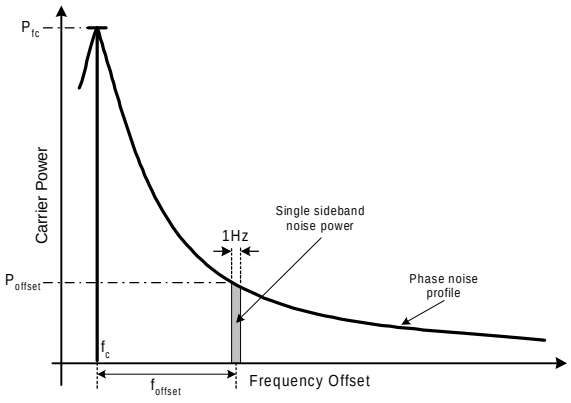

Figure 12 : Graphical description of phase noise.

The measure of phase noise is the difference between the absolute power level, P_{fc}, of the VCO at frequency f_c and the single sideband noise power, P_{offset}, at an offset frequency, f_{offset}, in a specified bandwidth (usually 1Hz). This gives the equation for phase noise at any given offset as

$$SSB\,Phase\,Noise(f_{offset}) = P(f_c) - P(f_{offset}) \qquad Equ.\ 13$$

with the units of the phase noise in dBc/1Hz (usually written as dBc/Hz) and $P(f_c)$ and $P(f_{offset})$ in dBm and dBm/Hz respectively. A comprehensive treatment of this extensive topic is given in [7].

Sources Of Noise From Within The Loop

Figure 13a) shows a simplified profile of the phase noise at the output of a PLL synthesiser.

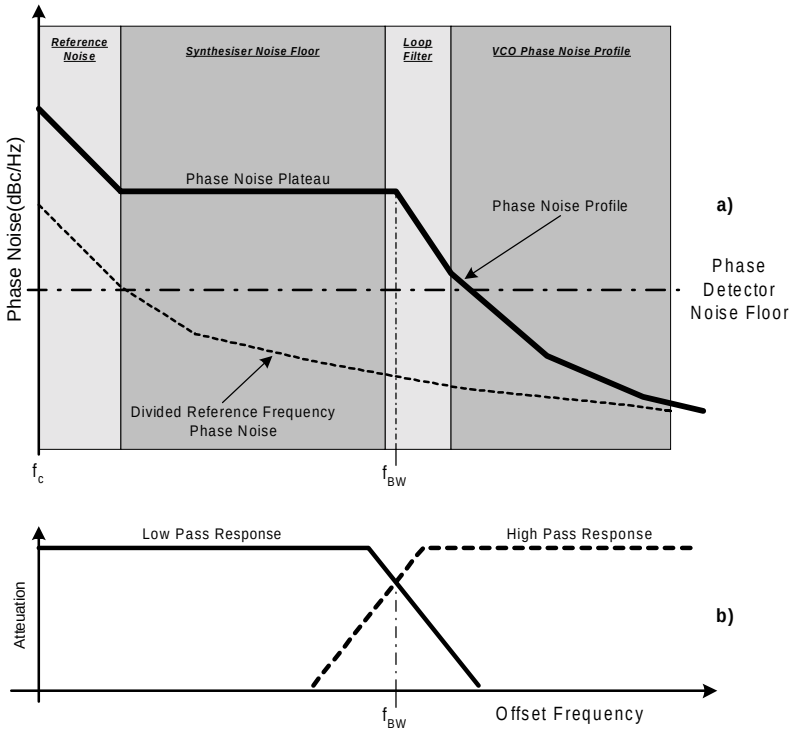

Figure 13 : Phase noise contributions in a PLL.

The action of the phase locked loop on phase noise is that of a low pass or high pass filter, see figure 13b), depending on whether the noise contributions are below or above the loop bandwidth respectively. At offset frequencies $\gg f_{BW}$ it is usual for the dominant noise contribution to be the VCO phase noise. At offsets $\ll f_{BW}$ the main noise contribution comes from the reference frequency source, although this is limited by the noise floor of the dividers in the loop. In the

region where the offset frequency is close to the loop bandwidth the noise levels are a combined contribution of both of these noise sources.

For synthesiser ICs with integrated dividers, the noise level can be normalised to an N value of 1 and a comparison frequency of 1Hz, called the phase noise index [8]. This index varies with each manufacturer and synthesiser. Some typical values of this index are given in table 1.

Synthesiser/Manufacturer	Phase Noise Index
LMX233x (Dual) / National Semiconductor	-211 [8]
LMX23x6 (Single) / National Semiconductor	-210*
ADF4212 (Dual) / Analog Devices	-217*

* : Measured using manufacturers evaluation PCBs.

Table 1 : Typical phase noise index values for some synthesisers.

The synthesiser noise level within the loop bandwidth can be approximated by

$$Phase\ Noise = (Phase\ Noise\ Index) + 20 \cdot Log_{10}(N) + 10 \cdot Log_{10}(f_{comp}) \qquad Equ.\ 14$$

where the phase noise is in dBc/Hz. Using equation 14 with N=(2.33GHz/500kHz)=4660 and f_{comp}=500kHz, the phase noise at 5kHz offset is predicted to be –86.6dBc/Hz The measured result is shown in figure 14 as –84.8dBc/Hz.

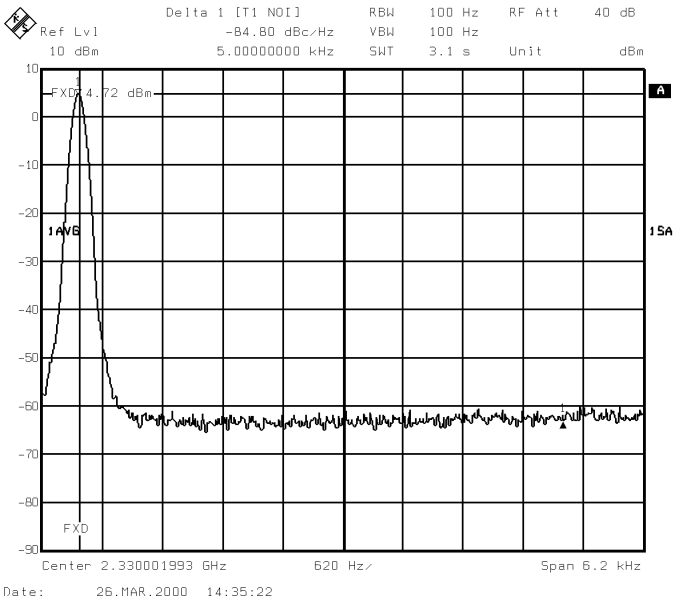

Figure 14 : Design example phase noise at 5kHz.

Other Noise Sources

There are other sources of phase noise that need to be considered when designing a PLL. One of the most common sources of noise is the power supply to the synthesiser. This can be caused in many ways, but most commonly are due to supply ripple and electric or magnetic coupling. Also, if there are any wire-wound components such as inductors or transformers in the design, these can act as mini antennas.

Correct PCB Layout of the PLL components relative to each other, and to other circuit areas, is critical to ensure good noise performance. For example putting a high performance synthesiser next to a switch mode power supply may prove disastrous.

Design Example Phase Noise Analysis

The measured phase noise of the example is given in table 2.

Frequency Offset (kHz)	Phase Noise (dBc/Hz)
1	-84.8
5	-84.8
10	-82.0
20	-84.5
50	-94.3
100	-105.1
500	-122.9
1000	-136.4

Table 2 : Synthesiser phase noise measurements.

The rms phase error contribution of the synthesiser over a specified bandwidth may be calculated using equation 15.

$$\varphi = \sqrt{\int_{f_{start}}^{f_{stop}} 10^{\frac{Y(f)+3}{10}} df} \qquad \textit{Equ. 15}$$

where

φ	:	RMS phase error (in rad. rms.)
f_{start}, f_{stop}	:	Offset frequency limits
Y(f)	:	Single sideband phase noise profile in dBc/Hz

Using equation 12, we find that the rms phase error for the synthesiser is approximately 0.91°. This is well inside the specification of ≤3°.

In summary this means that for an optimum overall phase noise profile the following design aims should be considered

- Use a good quality reference source.
- Try to set the loop bandwidth such that the level of the plateau in the noise profile meets the VCO phase noise at the same point.
- Use a low noise VCO.
- Try to reduce the overall division in the loop. As the noise within the loop goes up by $20*\text{Log}_{10}(N)$, keeping N low is important. For high frequency synthesisers requiring fine stepping consider architectures such as that in figure 1b) and c).
- Know your system's tolerance to phase noise and design only to meet this requirement. Trying to achieve excellent noise performance at all offsets will affect design time, and increase cost and complexity.
- Most importantly, ***look*** at the synthesised output on a spectrum analyser. The only real way to know what you've got is if you look at it !!

My Synthesiser Doesn't Work As Expected, Why?

After the synthesiser has been designed and built, there may be a few areas of the design which are not performing as required. Some of the more common problems are addressed below, with some of their possible causes, although it is always wise to check that the DC conditions are correct first, i.e.

- Are the power supplies correct and are they present on the synthesiser?
- Is the power supply current limiting or oscillating?

The synthesiser does not lock.

- Check that the VCO output is connected to the synthesiser RF input, and that the level is adequate.
- Check that the VCO is oscillating
- Check that the synthesiser is being programmed correctly.

The synthesiser does not lock in time.

- Is the bandwidth of the loop filter correct?
- Is the charge pump current set correctly?
- Do the capacitors in the loop filter have an excessive leakage current?
- As with the previous point, any residual flux left during soldering around the loop filter can also provide a leakage path for the current output of the charge pump.

The spectrum contains many spurious frequencies

- Are any inductors in the loop filter, VCO, etc. acting as antennas or "pick-ups" for high level RF signals in close proximity.
- Is the power supply to **all** the elements of the PLL well filtered and decoupled. Bench power supplies are notorious sources of noise. If possible, run the circuit from a battery supply.
- Is the synthesiser reference "clean"? Any spurious signals at the reference input will be subjecte d to a gain of 20*Log(N/R), modified by the loop filter shape.

The loop bandwidth is not as expected

- Have the loop components been calculated correctly? It is a common mistake to miss out factors of 2π (or add too many!!)
- If an active loop filter has been used, check that the op-amp does not introduce any poles which may alter the filter characteristic.
- Is the charge pump current set correctly?

The phase noise is higher than expected

- Is the phase noise of the synthesiser reference oscillator “clean”?
- Has the expected noise floor within the loop bandwidth been calculated correctly, i.e. using 20*Log(N)?
- Is the VCO oscillating correctly and not "multi-moding" (i.e. oscillating at more than one frequency at the same time)?
- If an active filter has been used, is it adding more noise than expected?
- The thermal noise contributions of large value resistors, used in the loop filter, can add to the overall noise of the synthesiser. Keep them as small as possible.

Summary

This paper has presented a simple overview of the basics of PLL synthesiser design, with particular reference to the use of integrated synthesiser ICs. Approximations of the frequency and transient responses and phase noise profiles have been shown and then applied to a design to show that they can produce a “real world” design. However, it should be noted that the topic of synthesisers is a vast one and it is far beyond the scope of this paper to cover all the design aspects. Every synthesiser design should be carefully assessed in its own right and careful calculations carried out to model any system critical areas on which the synthesiser characteristics may have an impact.

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